CMOS Applications

ENGR 453 – Lab 2
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Objective: To implement various types of CMOS gates and investigate their characteristics. Implement and explain the various applications of CMOS gates.

Components:
1 x CD4007
1 x CD4020
Miscellaneous capacitors : 3 x 33pF, 2 x 0.1μF, 1 x 0.01μF
Miscellaneous resistors : 1 x 1kΩ, 3 x 10kΩ, 7 x 100kΩ, 9 x 200 kΩ, 2 x 1MΩ, 1 x 22kΩ

General Procedures for PSpice

PSpice simulations were done for each part of the lab before actually performing the experiments. The PSpice simulations were used as an indication as to what should be expected when the experiments were actually performed.

All the PSpice simulations were done using the NMOS and PMOS PSpice model from experiment #3 of this lab manual.

General Procedures for Measurements

All the lab measurements were first measured using an analog scope. After these measurements were done, the lab was redone using a digital scope. Although this may seem redundant, the digital scope had an advantage over the analog scope, namely the digital scope is connected to a DAS system. This enables the capturing of data from the DAS to be inputted directly into the computer.

Basic CMOS gates

Three Input NOR Gate

The NOR gate was implemented using a CD4007. The CD4007 is a general purpose MOS array, consequently, there had to be some additional wiring to implement the NOR gate. Following the instructions shown in the lab manual, the CD4007 was wired as shown in fig. 1. The voltage used to power this circuit is 5V, which is the standard voltage for digital circuits.

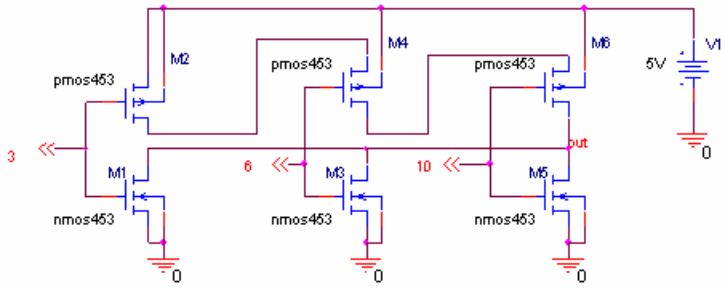

Fig. 1 – CD4007 wired as NOR gate

The function of the NOR gate is such that the output, labeled **OUT** in fig. 1, is high only if all the input, labeled 3, 6, and 10 in fig. 1, is low. The output is low for every other case, refer to table 1 for the NOR gate truth table.

3 6 10	Output		
	Ideal	Experimental	PSpice
0 0 0	1	1	1
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	0	0	0
1 0 0	0	0	0
1 0 1	0	0	0
1 1 0	0	0	0
1 1 1	0	0	0

Table 1 – Three input NOR gate truth table

The three-input NOR gate is simulated using the CD4007. Base on the schematic of the layout, the output, which is at pin 5, 8, and 12, would only be pulled up to V_{DD} if all the inputs, pin 3, 6, and 10 is grounded. This occurs since the NMOSs, which have the source and body tied to ground, would pull the output signal to ground if any if the NMOSs were turned on. Base on the operation of the NMOS, the NMOS would conduct only if the gate to source potential is greater than the threshold voltage of the NMOS. Consequently, the NMOS would be turned on if the gate, which are the input pins, are pulled up to V_{DD}.

Three Input NAND Gate

The three input NAND gate was implemented using a CD4007 wired as shown in fig. 2. From the circuit layout in fig. 2, the output would only become low if all the NMOSs were turned on. Since the three NMOSs are wired in series, if one of the NMOSs were to be off, the low signal cannot travel from ground to the output. Conversely, if any of the PMOSs was to be on, the output signal would the high. This is true since the PMOSs are wired in parallel, and would only require a minimum of one of the PMOS to be on to pull the output to high. The truth table for the three input NAND gate is shown in table 2.

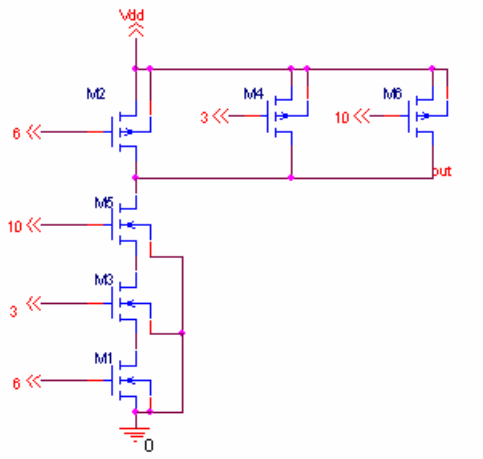

Fig. 2 – Three input NAND gate

3 6 10	Output		
	Ideal	Experimental	PSpice
0 0 0	1	1	1
0 0 1	1	1	1
0 1 0	1	1	1
0 1 1	1	1	1
1 0 0	1	1	1
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	0	0	0

Table 2 – Three input NAND gate truth table

Transmission Gates

The transmission gate is made using a PMOS and NMOS tied back to back as shown in fig. 3. The input signal is connected to the drain of the MOSs and the output is taken at the source MOSs. The transmission gate is turn on by the usage of G and NOTG. The signal G would turn on the NMOS if it is high, and since NOTG is just the complement signal of G, the PMOS would also be turned on. When the signal G is low, then both the PMOS and NMOS would be turn off. Fig. 4 show the plot of the transmission gate using an input signal of 2 V_{PP} @ 1 kHz.

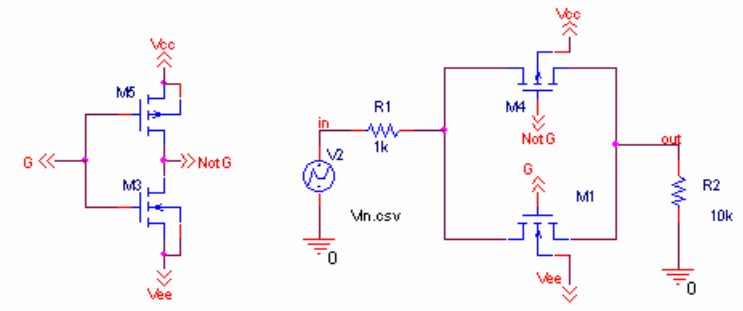

Fig. 3 – Transmission gate

From the plot shown in fig. 4, the output signal is slightly less than the input signal but still in phase. The cause for this attenuation of the output signal is due to the slight resistance of the MOS, $r_{ds(on)}$. With this resistance, the actual voltage seen at the output would be governed by the voltage divider formula, namely

$$V_O = \frac{R_L}{R_L + r_{ds(on)}} V_i \qquad \textbf{Eq. 1}$$

The transmission gate shown in fig. 3 is bi-directional, which mean the input and output can be interchanged. The reason this works, is the way the circuit is laid out. The MOSs are turn on by the usage of the signal N and NOTG. When the MOSs are turn on, this mean there is a conducting channel between the gate and the body. The channel does not cause the electrons to flow until there is a voltage potential applied at the drain and source of the MOS. This implies

the drain would be wherever the input signal is at and the source would be where the output signal is to be taken. To ensure this is correct, this part of the experiment was redone, but with the drain and source was interchanged. The output signal was the same as in fig. 4.

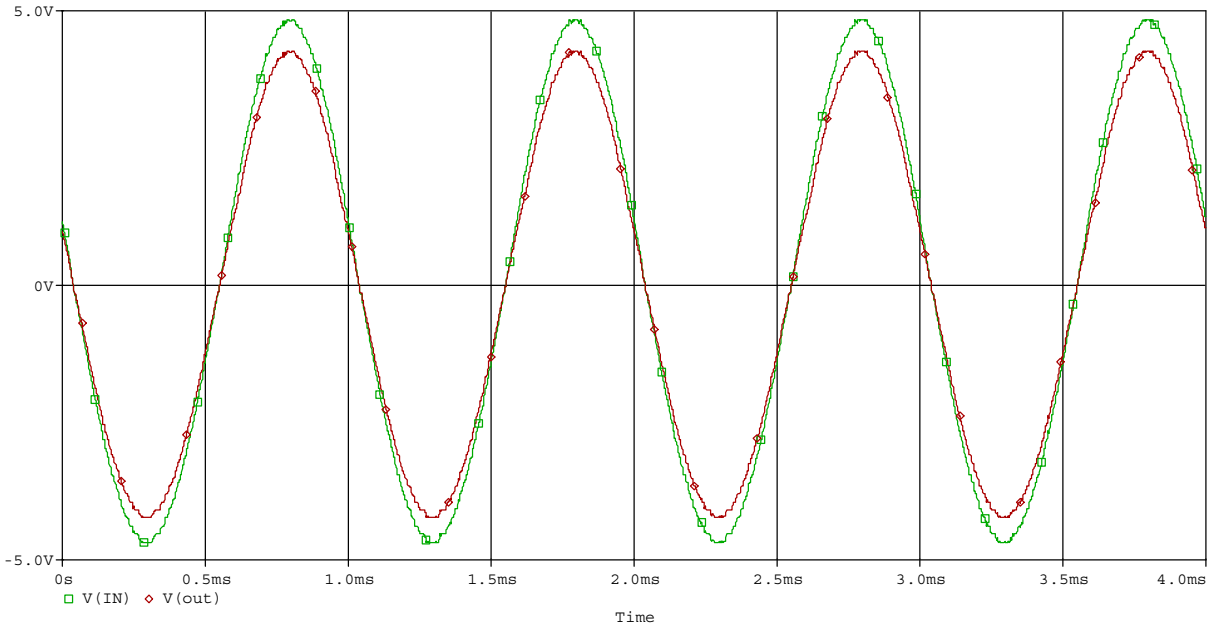

Fig. 4 – Input and output signal of a transmission gate

There is a limit to which the transmission gate will conduct. If the input voltage amplitude is raised greater than the power supply, clipping will occur. The simple answer to why this is true is because the output from a circuit cannot be more than the power supply used to power the circuit. To confirm this, using the same circuit in fig.3, the input voltage's amplitude was raised to 10 V_{PP} while maintaining the same frequency. As expected, the output waveform clips at approximately ±5V, which is the power supply, refer to fig. 5.

The transmission gate works by having the PMOS conduct during the negative cycle, while the NMOS conducts during the positive cycle. If one of the pins used in the transmission gate is left floating or connected to ground, only part of the wave will propagate through the transmission gate. To verify this theory, the pins that are consider the drain for the PMOS and NMOS, pin 12 and pin 3 of the CD4007 respectively, were disconnected. The signal was then viewed using the scope. The result from the scope, refer to fig. 6, showed that there was significant amount of clipping at the bottom of the wave when the PMOS was disconnected. This was as expected since the PMOS is supposed to conduct during the negative cycle of the waveform. Similarly, the output will have significant clipping at the top, if the NMOS is disconnected.

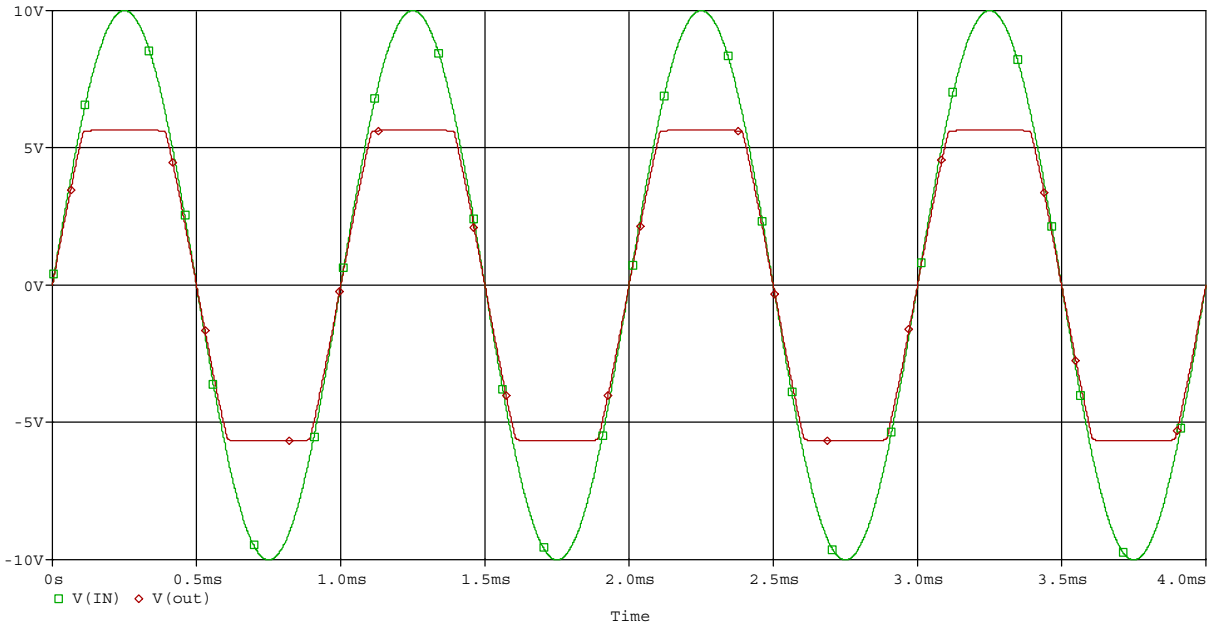

Fig. 5 – Transmission gate plot with V_{PP} = 10V

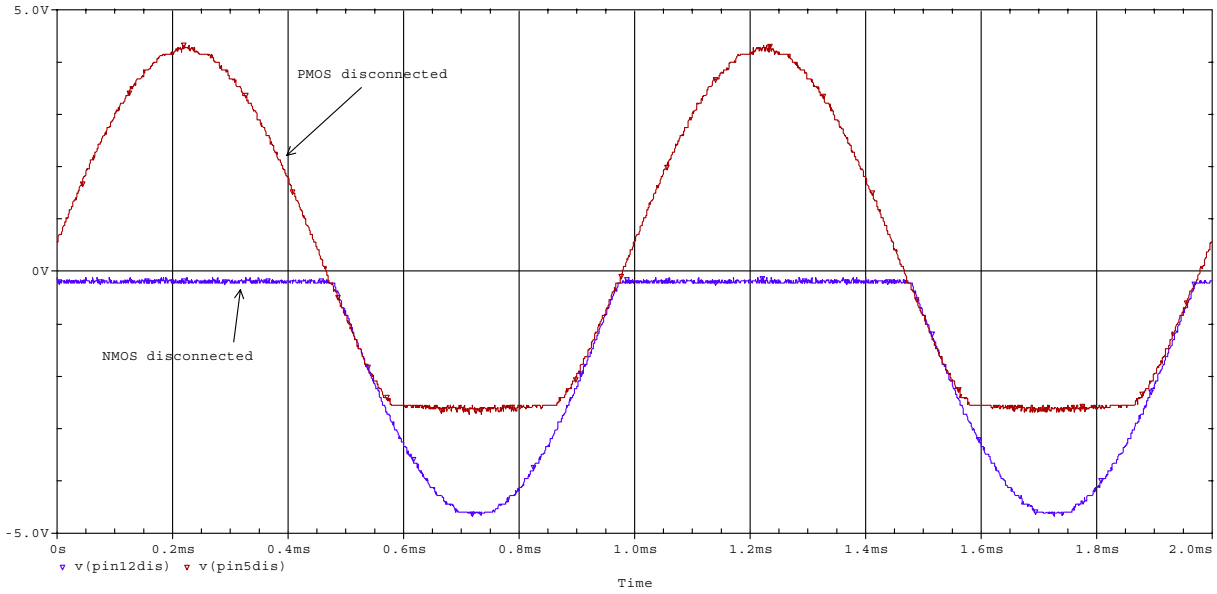

Fig. 6 – Transmission gate with some pins disconnected

Schmitt – Triggers

A Schmitt-trigger was synthesize using the CD4007. The circuit consists of three inverters in series, with a feedback resister from the second to the first inverter, refer to fig. 7. The feedback loop is used to ensure that there is no accidental change in output, for instance if the input signal had sudden spikes it would not cause the output to suddenly swing from high to low or vice versa.

The output at the second inverter tracks the input voltage. This means that if there is a sudden change in voltage at the input for a brief moment, this would not cause the output to change since the feedback resistor is feeding back some part of voltage from the second inverter. So, for the Schmitt-trigger inverter to change from a high to low state, the input voltage has to be less than V_{OL} for the inverters. Similarly, the input voltage will have to be less than V_{OH} for the Schmitt-trigger inverter to change from a low to high state. This implies that the V_{T+}, which is at the voltage level that is required to change from high to low, is V_{OL}. Then V_{T-}, the voltage required to change from a low to high state, is just V_{OH}. Using the results obtained from lab 3, V_{T+} would be 2.9V. V_{T-} would be 2.6V.

To verify this prediction, the VTC of the Schmitt-trigger was viewed on the scope, refer to fig. 8. Fig. 8 contains the data from both the PSpice simulation and the actual experimental data. The difference between the PSpice results and the actual data are very minute. From the VTC plot of the experimental data, the V_{T+} and V_{T-} are close to what was predicted.

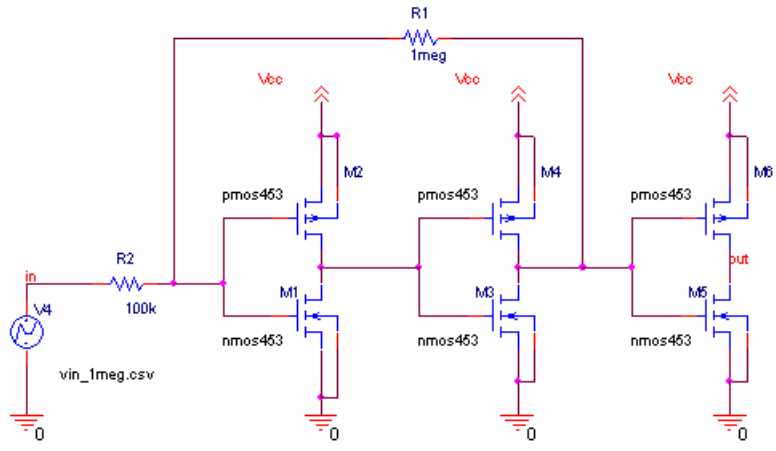

Fig 7 – Schmitt trigger

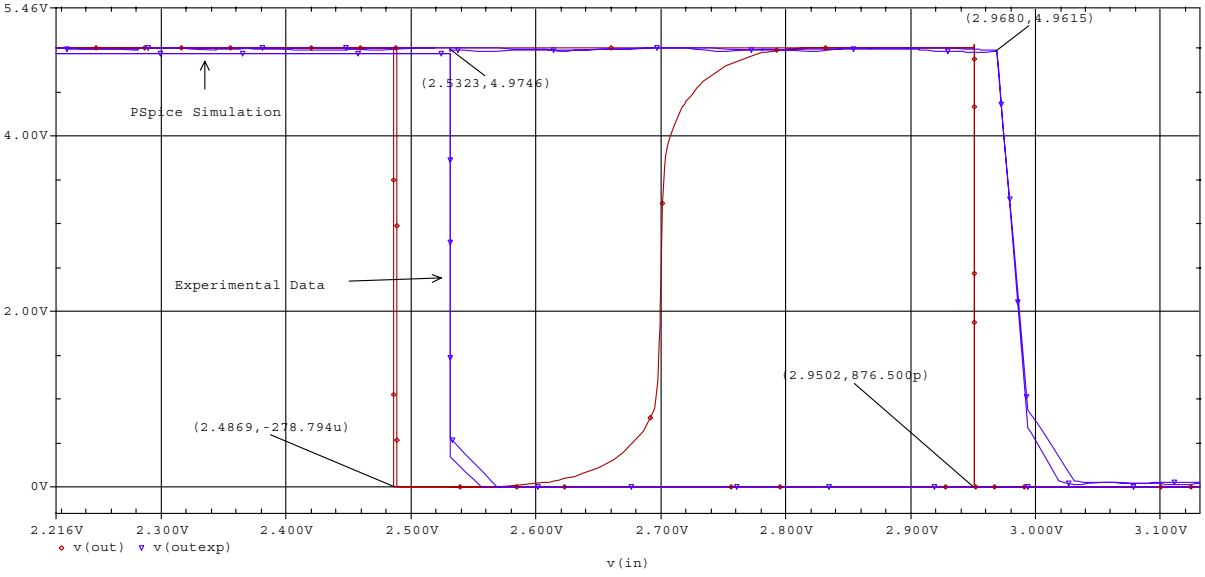

Fig 8 – VTC of the Schmitt-trigger inverter

The VTC of the Schmitt-trigger was plotted again, but with the feed back resistor equal 500 kΩ. The VTC now looks like fig. 9. Using these two graphs, it can be seen that the feed back equation is

$$V_F = \frac{R_F}{R_F + R_{in}} V_{DD} \qquad \textbf{Eq. 2}$$

And V_{T+} would then be

$$V_{T+} = V_M + V_F \qquad \textbf{Eq. 3}$$

And V_{T-} would be

$$V_{T-} = V_M + V_F \qquad \textbf{Eq. 4}$$

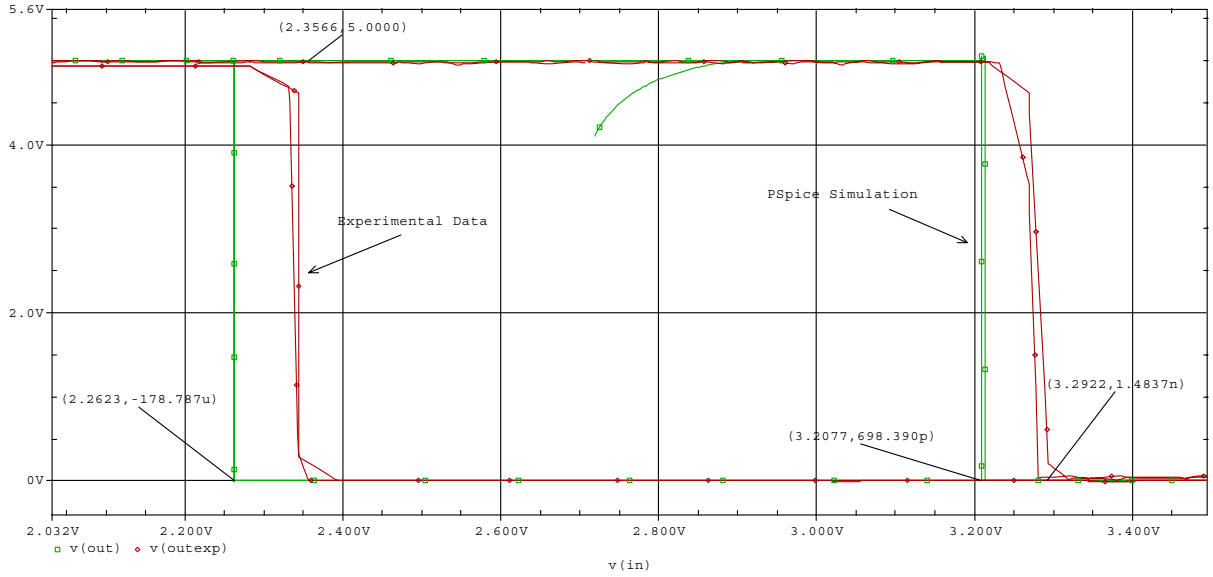

Fig. 9 – Schmitt-trigger inverter VTC with R_F = 500 kΩ

The experiment was performed again, but this time with V_{DD} = 10V. The plot is shown in fig. 10. Base on the measured value of V_M for V_{DD} = 10V in experiment 3, the V_{T+} and V_{T-} would have a different value than for V_{DD} = 5V. All the values for the Schmitt-trigger are summarized in Table 3 and Table 4.

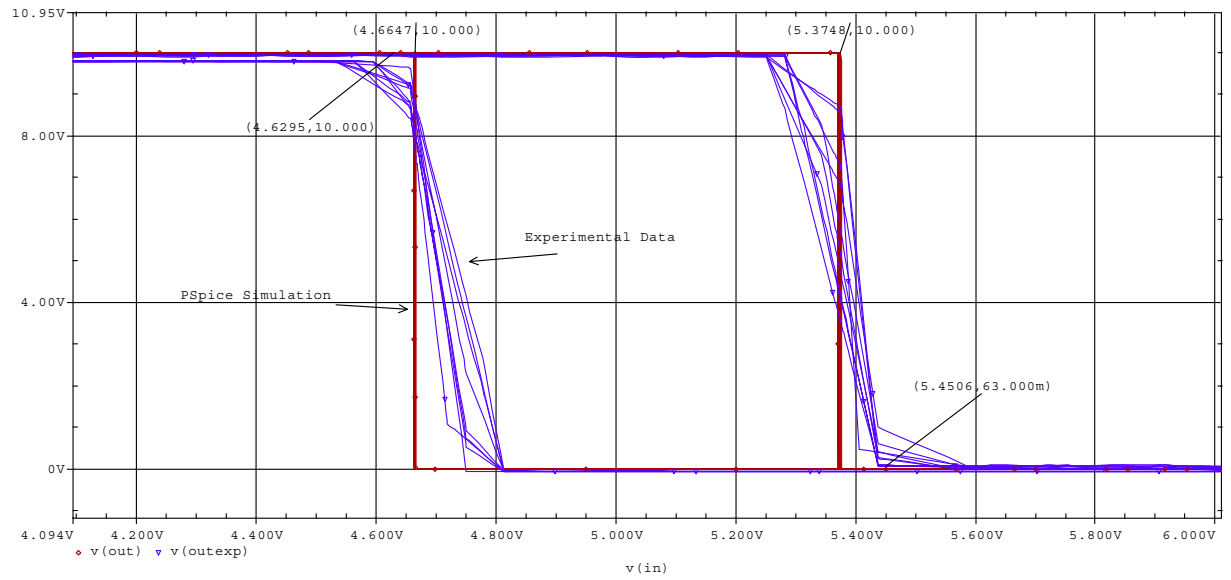

Fig. 10 – Schmitt-trigger inverter VTC with V_{DD} = 10V

	V_{DD} = 5V					
	R_F = 1 MΩ			R_F = 500 kΩ		
	Cal.	PSpice	Exp. Data	Cal.	PSpice	Exp. Data
V_F	0.45V			0.83V		
V_{T+}	3.05V	2.98V	2.95V	3.43V	3.21V	3.29V
V_{T-}	2.15V	2.53V	2.48V	1.77V	2.26V	2.36V

Table 3 – Data for Schmitt-trigger inverter with V_{DD} = 5V

	V_{DD} = 10V R_F = 1 MΩ		
	Cal.	PSpice	Exp. Data
V_F	0.45V		
V_{T+}	5.4V	5.35V	5.45V
V_{T-}	4.5V	4.66V	4.62V

Table 4 – Data for Schmitt-trigger inverter with V_{DD} = 10V

Astable Multivibrator using a Schmitt-trigger Inverter

Using a RC network with a Schmitt-trigger inverter, an astable multivibrator can be created, refer to fig. 11. The frequency is due to the RC time constant and $\pm V_T$ of the Schmitt-trigger inverter. Using this knowledge and with what was found in the previous section, $\pm V_T$ is found as

$$\pm V_T = \frac{R_f}{R_f + R_{in}} V_{DD} \text{ , where } R_f = 1\text{Meg and } R_{in} = 100\ \text{k}\Omega \qquad \textbf{Eq. 5}$$

Then using the standard form

$$\Delta t = \tau \frac{V_\infty - V_0}{V_\infty - V_1}$$, from Design with OP-Amp (Franco) **Eq. 6**

The waveform should be symmetrical, therefore only half the period need to be found

$$\frac{\Delta t}{2} = RC \ln\left(\frac{5+V_T}{5-V_T}\right)$$ **Eq. 7**

Using Eq. 7, the period was found as 18.04 μs, which translate to 27.5 kHz. The plot of the frequency is shown in fig. 12. From the plot, the actual frequency for the circuit is 18.6 kHz.

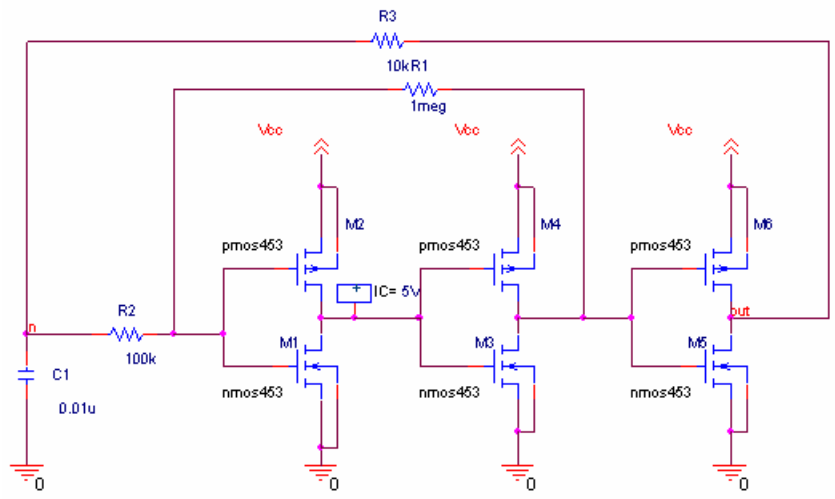

Fig. 11 – Astable multivibrator using a Schmitt-trigger

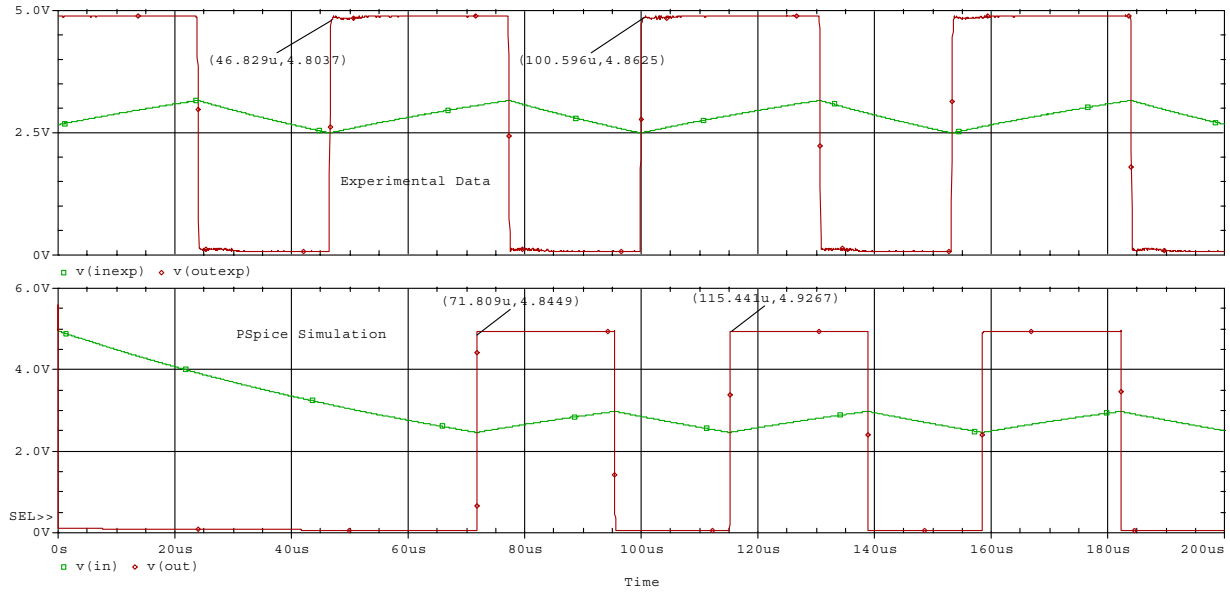

Fig. 12 – Frequency plot of astable multivibrator with R_F = 10 kΩ

From the plot shown in fig. 12, the input voltage rises when the output voltage is high, and vice versa. This can be explained base on the RC network. Assuming the output voltage, which is being feed back into the input is high, this charges up the capacitor to the voltage V_{T-}. But once the capacitor charges up to V_{T-}, it will force the output voltage to become low. Since at this point the output is low, this will force the capacitor to discharge. Once the capacitor voltage discharges to V_{T+}, it will force the output voltage to become high, which will then charge the capacitor to V_{T-}. This constant charging and discharging will cause the output voltage to oscillate between V_{DD} and ground potential.

The frequency of the astable multivibrator can be change in two ways; one way is to change the V_T of the Schmitt-trigger inverter. This can be accomplished either by increasing or decreasing the power supply to the Schmitt-trigger inverter or by changing the internal feed back network in the Schmitt-trigger inverter. This is not practical since CMOS technology is usually power by 5V and there is no practical way to change the internal wiring of the Schmitt-trigger. The second way is to change the RC constant of the RC network. This way is preferred since the Schmitt-trigger used in this lab is base on the CMOS technology.

To increase the frequency of the astable multivibrator, the best way would be to decrease the RC constant. And to decrease the frequency of the astable multivibrator, the best way would be to increase the RC constant. In order to confirm this theory, the frequency of the astable multivibrator was plotted again, but using a bigger resistor, which means a larger RC time constant, refer to fig. 12.

From the plot in fig. 13, the frequency is 10 kHz, which is smaller than the frequency found in fig. 12.

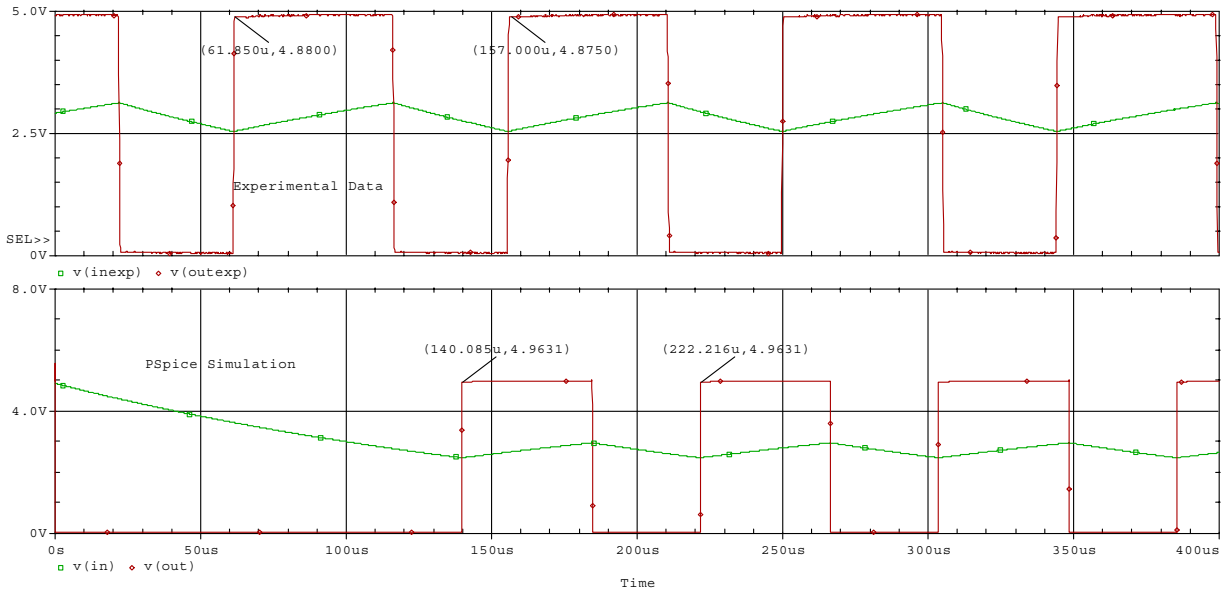

Fig. 13 – Frequency plot of astable multivibrator with longer RC constant.

Although it is impractical to change the internal feed back network of the Schmitt-trigger inverter, this was done to prove that the frequency of the astable multivibrator can be change by

changing the feed back network. The frequency of the astable multivibrator was plotted again, but this time, the internal feed back resistor, R_F, was changed to 500 kΩ while maintaining the same RC network used to plot fig. 14. With this change, it was expected that the frequency would decrease. This is because the Schmitt-trigger inverter's output would only change if the input voltage is greater than V_T. By changing the R_F from 1 MΩ to 500 kΩ, the V_T of the inverter has increase. This implies it would take longer to change the input voltage from V_{T+} to V_{T-}. This would then translate to a smaller frequency.

Base on the plot shown in fig. 14, the frequency is 5.6 kHz, much smaller than the frequency found in the previous section.

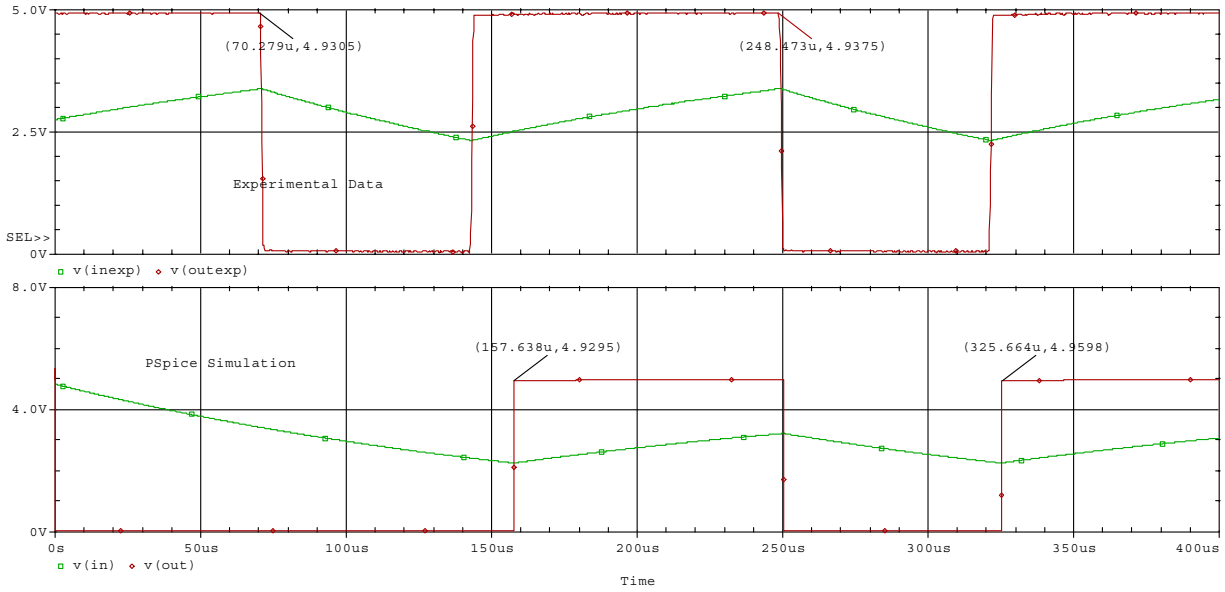

Fig. 14 – Frequency plot with R_F = 500 kΩ

The RC network present in the astable multivibrator is to create a controllable frequency vibrator. But even if the capacitor was removed, the circuit would still vibrate. It can be seen from the circuit in fig. 10 that with the capacitor removed, the circuit becomes a self-oscillating ring counter. The output is feed directly back into the input. Now, based on the operation of a inverter, whenever the input is low, the output is high, but since the output is connected back to the input, this will cause the input to change from high to low. This would then cause the output to change from high to low. The only way to control the frequency of oscillation would be to change the V_T of the circuit. The frequency of oscillation is also be governed by the time propagation delay across each of the inverters internally. So, if the time delay through the inverters is small, the frequency will be fast. Conversely, if the time delay is long, the frequency will be slow.

Multivibrators

The circuit in fig. 15 uses a NOR gate and an inverter to implement a multivibrator. The NOR gate yields a high output only when both inputs are low; if at least one of the inputs is high,

the output will be low. Under normal conditions, V_{Pin1} is low and the capacitor is in steady state, so $V_{Pin10} = V_{DD}$ due to the pull-up action of the resistor, and $V_{Pin12} = 0$ because of the inverter. This implies the voltage across the capacitor will be zero.

The arrival of the pulse at the input of the NOR gate will cause V_{Pin1} to pull to low. Now, the capacitor voltage cannot change instantaneously, which would make V_{Pin10} go to low, causing V_{Pin12} to be high. This action causes the capacitor to start charging. As soon as V_{Pin10} reaches V_T, the inverter changes state, causing V_{Pin12} to change back to low. In response to this, the NOR gate forces V_{Pin1} to high. This chain effect would occur at the pulse wave arrives at the input.

With this in mind, the circuit was done using PSpice and implemented in the lab. Fig. 16 show the result from the of the pulse wave arriving at the input.

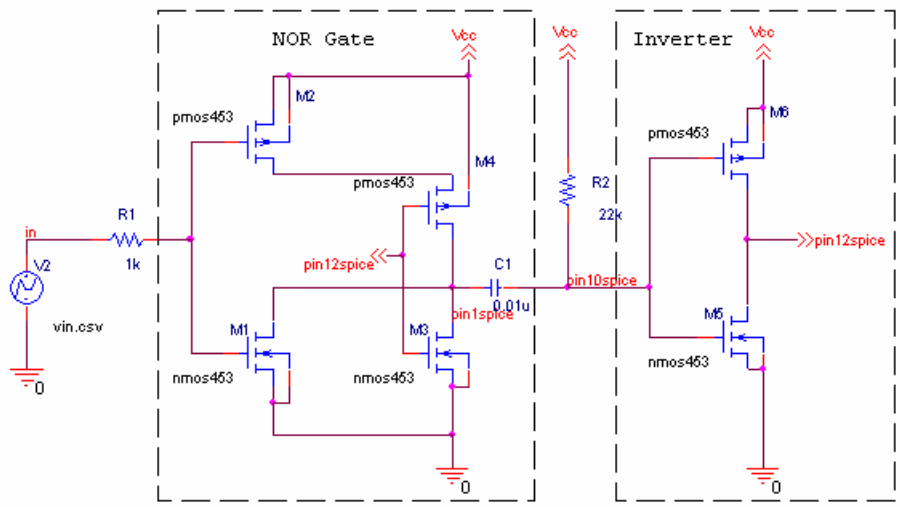

Fig. 15 - Multivabrator

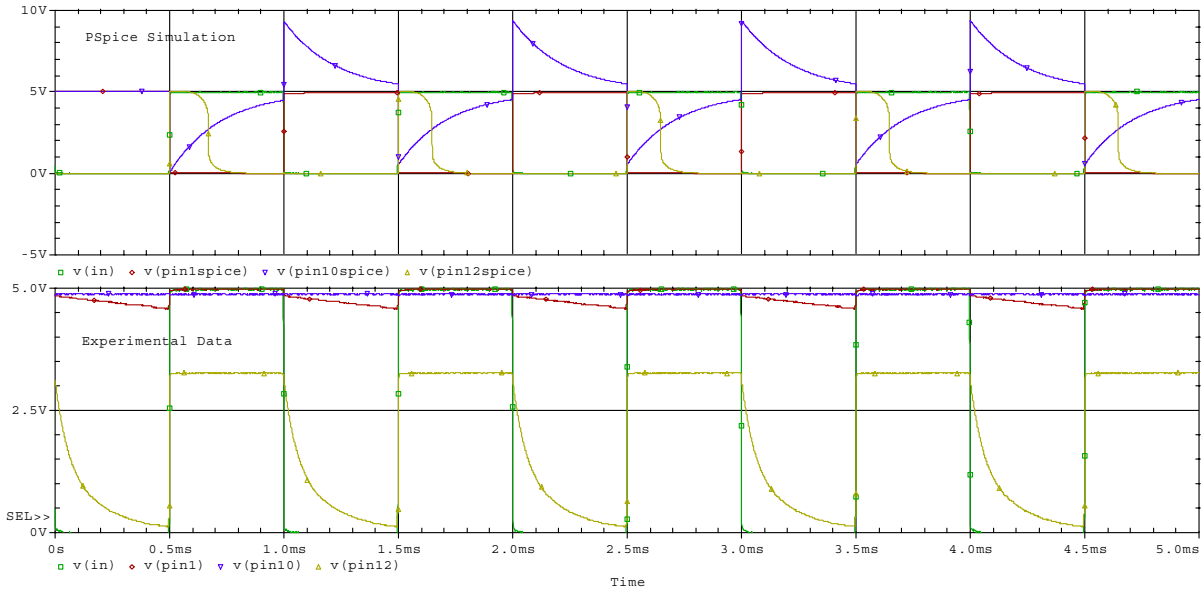

Fig. 16 – Multivibrator wavforms.

Using eq. 6 and the knowledge that there is RC constant affecting the circuit, the period of the output wave is

$$T = RC \ln \frac{V_{DD}}{V_{DD} - V_T} \qquad \textbf{Eq. 8}$$

From this equation, the frequency of oscillation is found to be 5.9 kHz roughly half of the frequency of the input waveform.

The circuit shown in fig. 15 can be configured to become an astable multivibrator by hardwiring the NOR gate to ground and placing a feed back network in the circuit, refer to fig. 17. The operation of this circuit is the same as the multivabrator, but now the RC constant is actually the $R_{eq}C$, where R_{eq} is the parallel resistance of the 100 kΩ and the 1 MΩ resistor. Also, since the output is being feed back into the input of the inverter, the inverter acts similar to a Schmitt-trigger. Using the same procedure in finding the period of the multivibrator with eq. 7 and eq. 8, the frequency is calculated at 1.4 kHz. The actual data was plotted and is shown in fig.18. From fig. 18, the frequency measured is 968 Hz

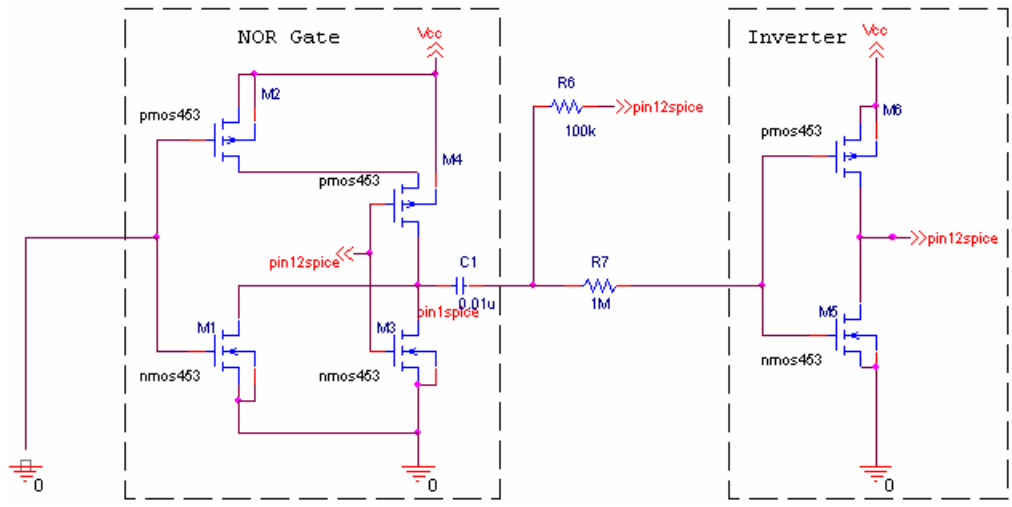

Fig. 17 – Astable multivibrator

. The astable multivibrator shown in fig. 17 can be turned into a "touch activated oscillator" by the means of a pull up resistor connected to the input of the NOR gate. The pull up resistor has the value of 10 MΩ. If a conducting path to ground is established, i.e. touching the input of the NOR gate with a finger, the oscillator will begin to oscillate. Although in principle this should work, this circuit did not performed as expected. Even when a conducting path to ground was formed, the circuit did not oscillate. We believe the lab members did not have enough resistance to form the path. Because of this, we used a simple wire, which act as a simple switch, to form a conducting path to ground. This configuration works.

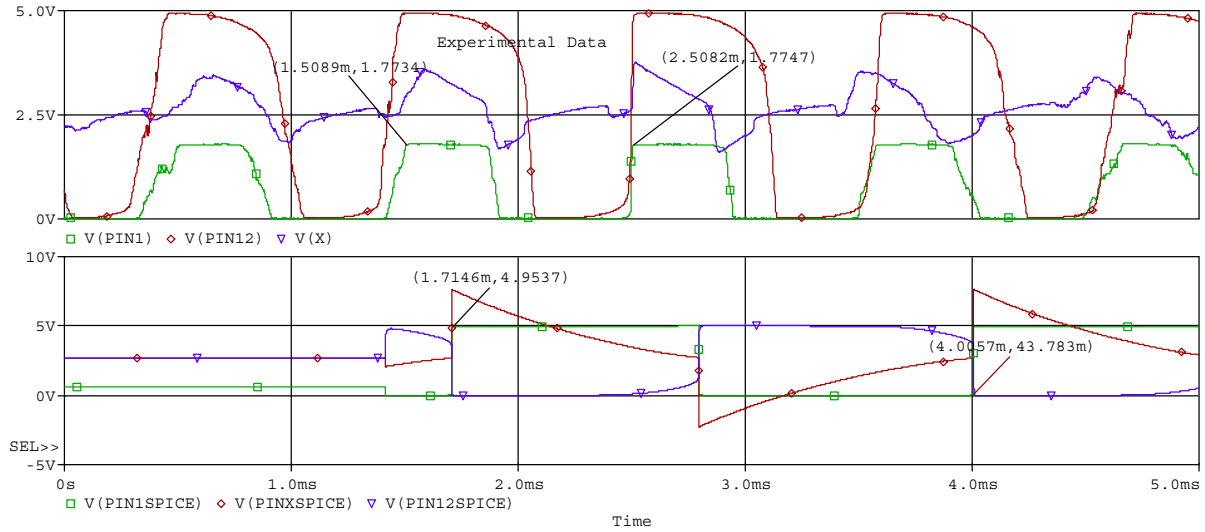

Fig. 18 – Astable multivibrator

Amplifier

Using just an inverter and two resistors, a negative feedback circuit was implemented, refer to fig. 19. The capacitor is there to act as a DC couple. The DC couple is needed since there is a feed back from the output when there is no input applied, specifically V_M. The reason the value is V_M is because with the input left floating, the inverter tries to determine the output voltage state, either high or low. But since the circuit is in a state of instability, the output will switch back and forth.

The circuit was initially investigated with the inverter powered, but with the input node left floating. The voltage found at the output was 5.01V or approximately V_M. This value represent the DC offset that is introduce to the circuit.

The experiment was done again, with the input node connected to a sinewave with a V_{PP} of 1V @ 1 kHz. The output voltage had a V_{PP} of 2.8197V @ 1 kHz, but 180 out of phase with respect to the input voltage, refer to fig. 20.

Base on the plot, it appears the amplifier have a gain of approximately 3V/V. Looking at the circuit, and without doing any hand calculation, it appears the gain of the amplifier is $-(R_2/R_1)$+DC offset.

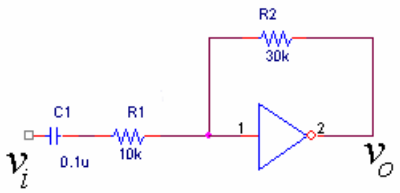

Fig. 19 – Inverting amplifier

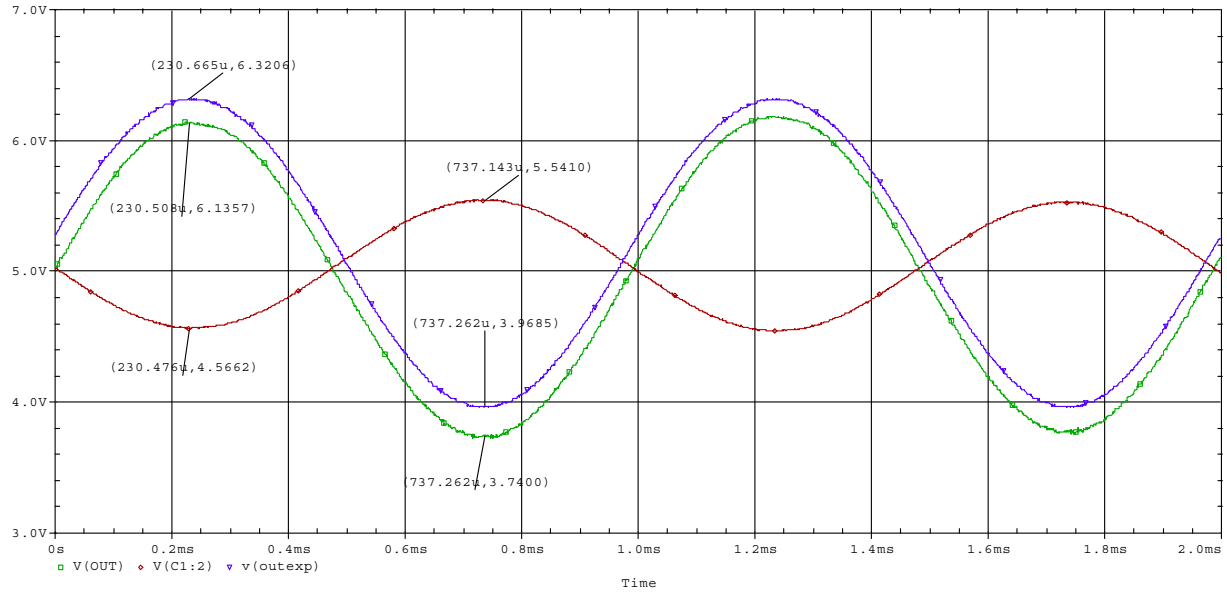

Fig. 20 – Amplifier using inverter

D/A Converter.

A D/A converter was build using a Schmitt-trigger astable multivibrator connected to the input of a 14 stage binary counter, a CD4020. Using a terminology of the MSB as being in the right most bit, pin 15 of the CD4020 in fig. 21, and the LSB as the left most bit, pin 7 of the CD4020, the function ability of the D/A converter was investigated.

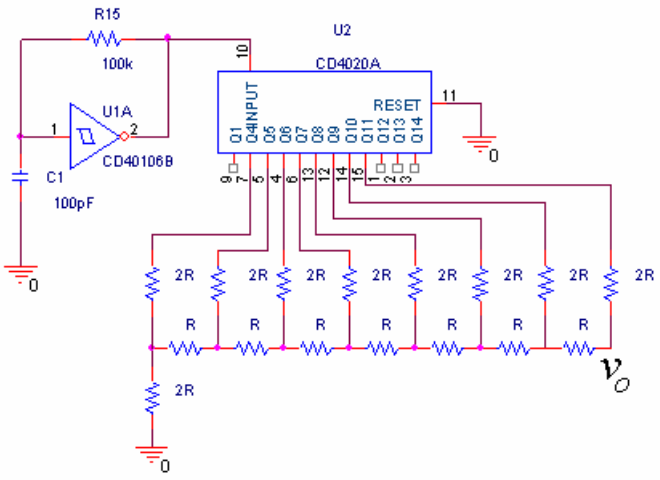

Fig. 21 – D/A Converter

The function of the D/A converted was investigated first with enabling only one bit at a time. Bit 7 through bit 4 are shown in fig. 22, the other bits are not shown since they did not have a very good output waveform, specifically there was too much noise to really clearly indicate the amplitude and the frequency of the waveform. To view the output of each bit, only one bit was enable, tied to the counter, while the other bit tied to ground. From the output show, the MSB has the highest amplitude with the smallest frequency while the LSB have a lower amplitude and a smaller frequency.

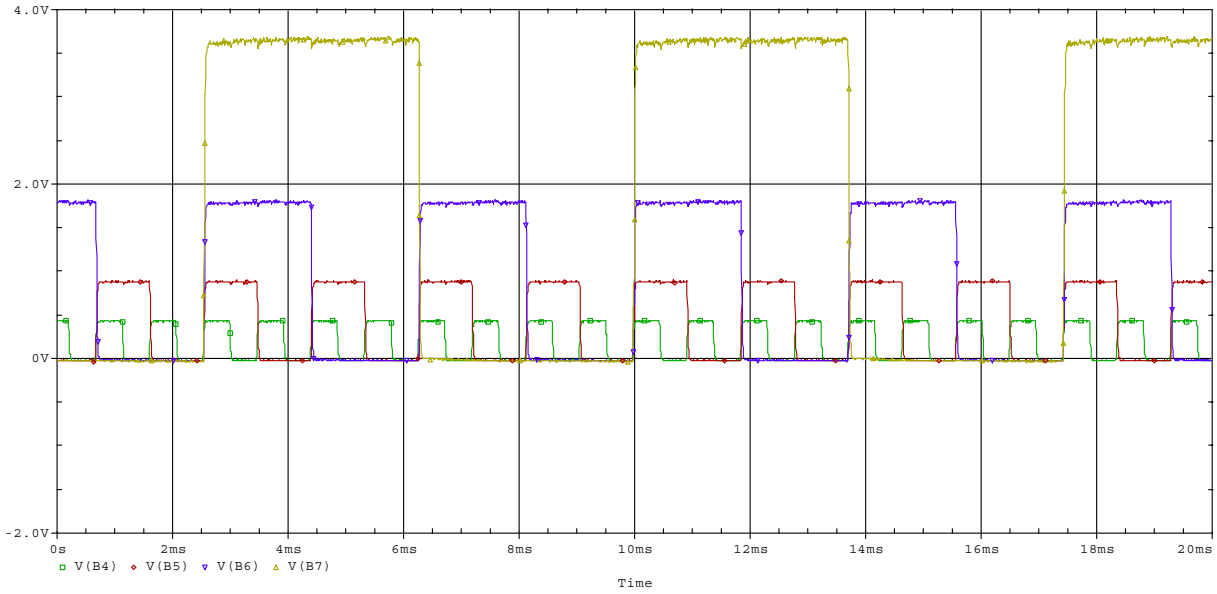

Fig. 22 – D/A output

The amplitude changes because of the resistive network ladder. To show how the resistive network affect the output, a detail analysis will de done with B7 enable and the other bits grounded. With the other bit grounded, it is a simple matter to find the equivalent resistance seen from B7, which is 2R. The output could then be found using a voltage divider formula. From this, the output would be (R/2)*B7. Using the same approach, the other voltage can be found. The other voltage would be smaller as the bit number decreases.

The frequency increases because the output is taken from a binary counter. From the previous lab, lab 3, we have demonstrated that the counter can be used as a frequency divided. Now base on the data sheet provided by Fairchild Semiconductor, refer to the data sheet accompanying this report, it appears that the LSB is f/16 with the frequency being divided by a smaller amount on the MSB.

Since we are using this circuit as a D/A converter, it would be instructional to see how the output would look like if more than one bit was enabled. Following the instructions provided in the lab manual, three graphs were plotted: one plot with B7 and B6 enable, one plot with B7, B6, and B5 enabled, and finally one plot with B7, B6, B5, and B4 enabled, refer to fig. 23.

From the graph, as more bit is enable, there are more steps to the graph. This can be easily explain using the superposition principles. The superposition principle can be used since the only components that are used in this circuit resistors. Resistors are linear element and the superposition principle can be used only if the elements used in the circuits are all linear. Looking back at the plot shown in fig. 22, if the graph for B7 and B6 are added together, the graph would be a step with. Using PSpice, a plot was done by adding the output waveform of B7 and B6, refer to fig. 24.

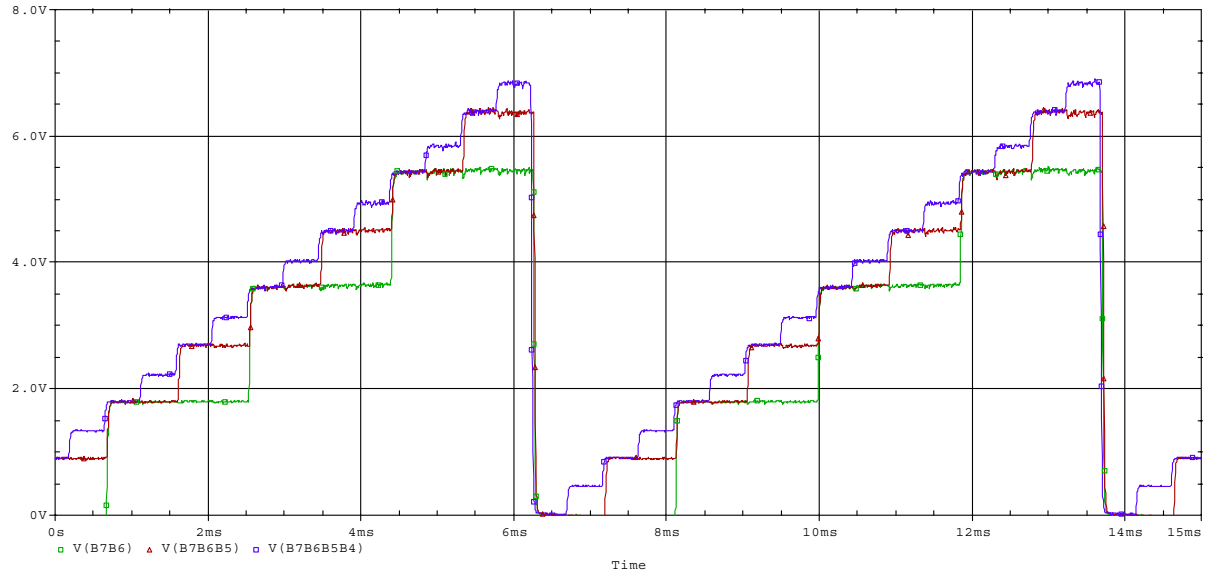

Fig. 23 – D/A converter with more than one bit enabled

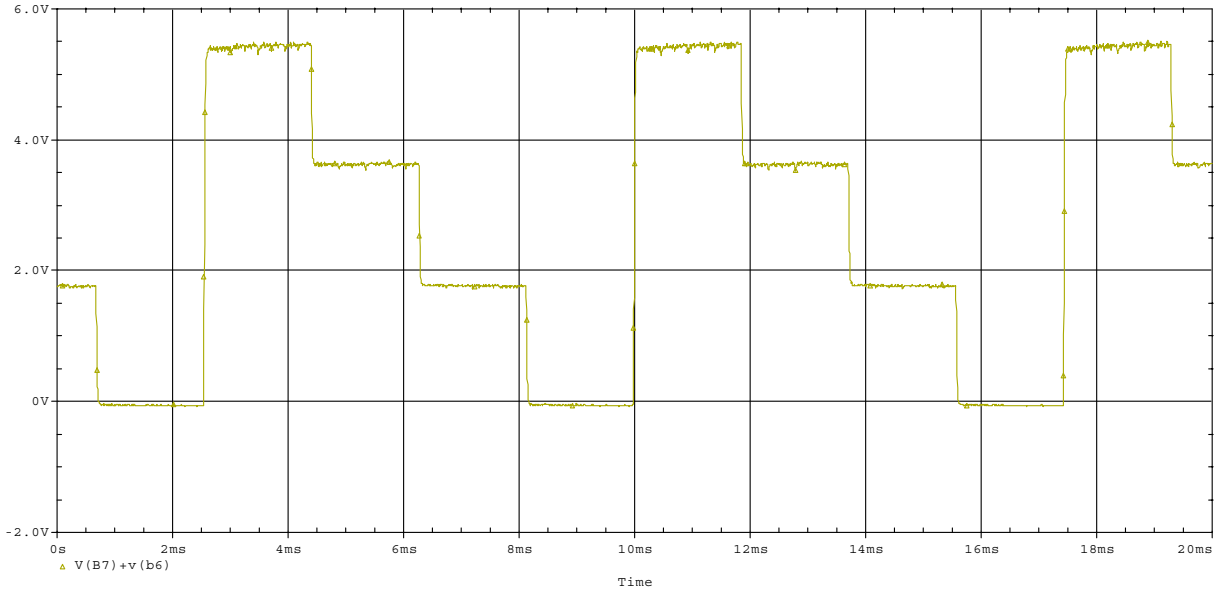

Fig. 24 – Output with B7 and B6 added together.

From this two experiment, it is easily seen that as more and more bits are enabled, there would be more and more steps to the waveform. But there would be a point in which adding more bits would not make sense. Why? From a logical stand point, as more and more bit are enabled, more and more steps should appear, but also the spacing between the steps would decrease. So if to many bits are enabled, the spacing would be so small that it would look like a sawtooth waveform.

This D/A circuit would work with most voltage. The counter does not affect the frequency of the output if the input frequency remains the same. But if the voltage of the input is decrease, the output voltage would decrease. This is so because the output for each bit is goes

through a voltage divider. To verify this experimentall, the power supply, V_{DD} was lowered from 10V to 5V. The graph was plotted again, but with only the output for B7, B6, B5, and B4, refer to fig. 25. The lower bits were not plotted because there was too much noise making the amplitude and frequency immeasurable.

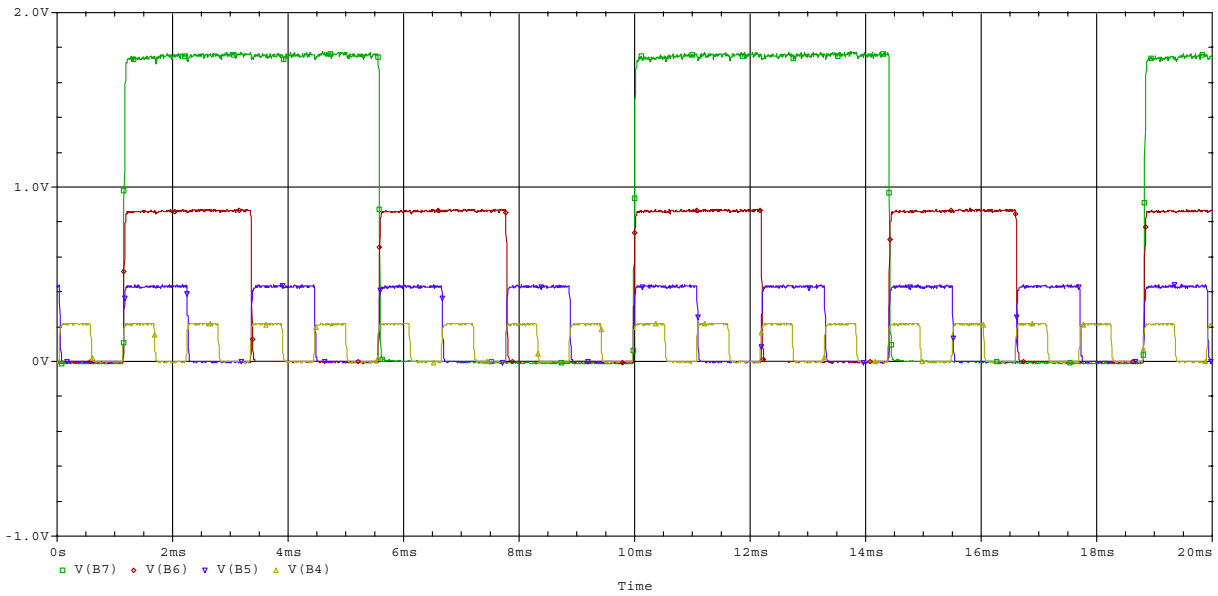

Fig. 25 – D/A converter with V_{DD} = 5V

There are several way to change the step size at the output, one is to connect the output to different Q on the counter, this causes the frequency of the input to be divided by a different amount or by changing the input frequency. The input "clock" is a Schmitt-trigger astable multivibrator, a multivibrator whose frequency is dependent on the RC constant of the circuit. So if the capacitor value or the resistor value was to be changed, the output frequency would change, but not he amplitude if the power supply remain the same.

This D/A is providing to have more used than originally thought. But so far the investigation have only been concern with only one bit enabled at a time and with a succession of bits enabled. It would be interesting to see how the output would look like if the MSB was grounded while the LSBs were enabled. The experiment was performed; one with B7 grounded and one with B6 grounded. The waveforms are shown in fig. 26.

Base on the output, it appears that the D/A would produce a steps at the waveform only if the MSB is enabled, specifically B7. Without B7 enabled, the output does not make sense. There is no way to explain what it does.

So far, to enable a bit is to connect it to the counter, while to disable a bit means to ground the bit. Looking at the circuit, it should seem logical that to disable a bit, the bit can be either grounded or left floating. This is not so. Since the output is dependent on the resistive network and the voltage divider that is formed when the disable bit are grounded, the output voltage would be different if the bits was left floating. To clarify this, let's assume B7 was connected to the counter while B6-B1 was connected to ground and B0 was left floating. Using

simple electronics analysis, the equivalent resistance seen from the output would be approximately 1.99R. Using the voltage divider formula, the voltage would be less than with B0 grounded.

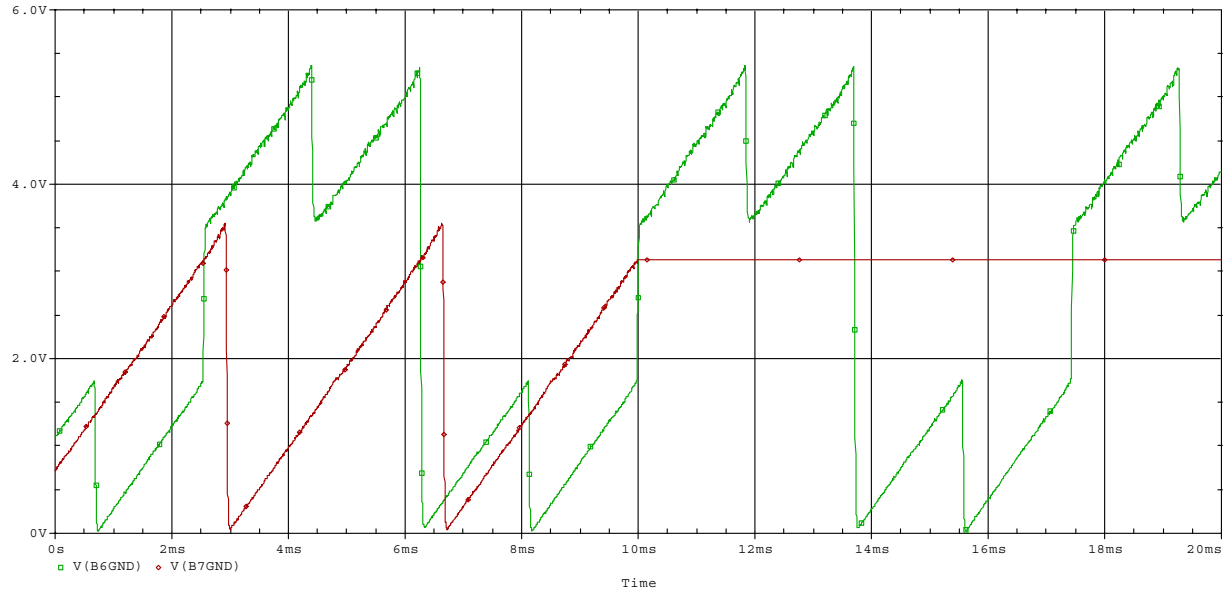

Fig. 26 – MSB grounded with LSB enabled

Conclusion:

CMOS technology is a very versatile thing. Using just CMOS, a variety of circuits can be build, both for digital and analog operations.

The simplest application that can be build using CMOS are basic logic gate. Each logic can be broken down into two components, a pull up network and a pull down network. The pull up network is used to pull the output to the high state while the pull down network is used to pull the output to the low state.

Transmission gates can be build by using a PMOS and a NMOS transistor put back to back. The transmission gate allows and analog signal to pass through with very low degradation. The transmission gate can be used as a buffer since the resistance seen by the MOS are very high. Although the operation of the transmission gate can also be accomplished by the used of an op-amp configured in the voltage follower configuration, it has the advantage of having fewer components than the op-amp. The disadvantage is the output is not exactly similar to the input signal. This is cause by the low resistance, $r_{d(on)}$, seen by the signal when is transmitting through the MOS. There is also an disadvantage of the voltage that can be used with the transmission gate. Specifically, the body of the NMOS should be connected to a more negative voltage than the gate, this allows the signal to travel through easier. But for this to be true, this would mean the usage of two power supply.

A Schmitt-trigger inverter is useful as a buffer. If the input signal contains a sufficient amount of noise, a regular inverter should not be used. A regular inverter would change the output state according to the input state. So if the input signal has a log of sudden spike due to noise, the output would also have sudden spike. The Schmitt-trigger inverter overcomes this by being immune to noise. The only time the output state of the Schmitt-trigger changes is when the input signal is greater than V_{T+} and less than V_{T-}.

A simple astable multivibrator can be constructed using a simple RC network with a Schmitt-trigger inverter. The frequency of the multivibrator is primary determined by the RC value of the network, as such it is an easy matter to vary the frequency of the multivibrator. Although the frequency can be varied by the value of RC network, it is also possible to change the frequency by increasing or decreasing the V_T of the Schmitt-trigger inverter. This is impractical since the Schmitt-trigger inverter normally used would be in an IC package and it would be very hard to change the internal feed back network.

In addition to an astable multivibrator, a gated astable multivibrator can be design using CMOS technology. The gated astable multivibrator used in this lab consisted of a NOR gate, an inverter and a RC network. Unlike the astable multivibrator, this multivibrator can be controlled either by using a switch or by using a finger. As if the Schmitt-trigger astable multivibrator, this multivibrator's frequency is also controllable by the mean of changing the value of the RC network.

A simple inverting amplifier can be implemented by the use of two resistor and an inverter. This amplifier has a big disadvantage, which is there is a DC offset at the input node.

This is not desirable in an amplifier. The DC offset should be zero. The only time a DC offset should be present is when it is intended to be there. For the amplifier in this lab, the DC offset is approximately the V_M of the inverter, which about 5V. So to have a large swing for the output, the power supply would have to be huge.

The final application done was a D/A converter using a Schmitt-trigger astable multivibrator as a clock. The output was implement using a 14-bit binary ripple counter connected to a 2R-R resistive network. The output observed relied on two component: the frequency of the clock and the value for the resistive network. Since the 2R-R resistive network are operating in the linear region, it is very easy to derive the equations to relate the output to the input.

Discussion

This lab as a whole was pretty interesting but too much emphasis was place on deriving equations. We spend quite a big amount of time trying to figure out the equations for the multivibrator. It was a little easier for us since there was one member in the group who had took ENGR 442, which was a class for op-amp. That class included some lecture on how to derive equations for multivibrator.

We did not understand the need of the D/A converter experiment. Although we know how the Schmitt-trigger astable multivibrator worked, we did not know how the CD4020 was supposed to work. All we learn from this part was that the output results in pulse waveforms with various frequency and amplitude. Other than that, not much.