ENGR 301 – Electrical Measurements

Experiment # 6: Logic Circuit Characteristics and Simple Logic Gates

Objective:

To characterize BJT and CMOS *inverters*. To investigate simple *logic gates*. To compare *measured* and *simulated* logic circuits.

Components:

2 × CD4007UB MOSFET Arrays, 2 × 2N2222A *npn* BJTs, 4 × 1N4148 *pn* diodes, 1 × 0.1 μF capacitor, and miscellaneous resistors: 1 × 1.0 kΩ, 1 × 3.0 kΩ, and 1 × 10 kΩ (all 1%, ¼ W).

Instrumentation:

A bench power supply, a signal generator (triangle wave), a digital voltmeter (DVM), and a dual-trace oscilloscope.

References:

1. Sedra, Adel S., and Smith, Kenneth C., *Microelectronics*, 4th Ed, Oxford University Press, 1997.
2. Roberts, Gordon W., and Sedra, Adel S., *SPICE*, 2nd Ed., Oxford University Press, 1997.

Theoretical Background:

The most basic logic circuit is the *inverter*. To build a complex digital system we need more sophisticated logic circuits such a NAND and NOR gates, flip flops, encoders/decoders, registers, and memories; however, when it comes to the study of electrical properties, the basic inverter, in spite of its simplicity, is fairly representative of most logic circuits, so we find it appropriate to investigate it in proper detail.

As shown in Fig. 1, the inverter is powered between V_S (typically 5 V) and ground. Circuit behavior is best visualized in terms of the *voltage transfer curve* (VTC), which represents the plot of v_O versus v_I. Figure 2 shows the idealized VTC of an inverter. For $v_I < 0.5V_S$ the circuit gives $v_O = V_S$, and for $v_I > 0.5V_S$ it gives $v_O = 0$ V.

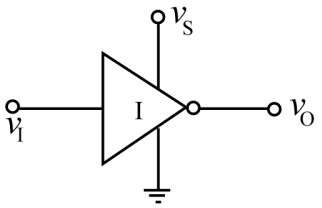


Fig. 1 - Logic inverter.

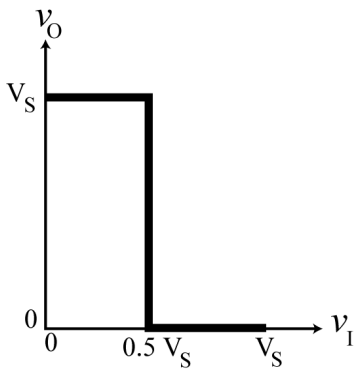


Fig. 2 - Idealized voltage transfer curve (VTC).

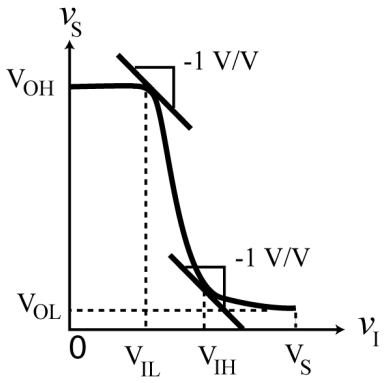


Fig. 3 - Practical VTC.

The VTC of a practical inverter will depart from this idealized VTC, and will look more like that of Fig. 3. Here we observe that as long as v_I is *sufficiently LOW* (i.e. near 0V), the inverter will give $v_O = V_{OH}$, where V_{OH} represents the HIGH output level, and as long as v_I is *sufficiently HIGH* (i.e. near V_S), the inverter will give $v_O = V_{OL}$, where V_{OL} represents the LOW output level; note that V_{OL} and V_{OH} are not necessarily equal to 0 V and V_S.

The departure of a practical VTC from the ideal is characterized in terms of the *noise margins*, defined as

$$\mathrm{NM}_L = V_{IL} - V_{OL} \qquad (1a)$$

$$\mathrm{NM}_H = V_{OH} - V_{IH} \qquad (1b)$$

where V_{IL} and V_{IH} are the values of v_I corresponding to the points of the VTC where the slope is -1 V/V. Physically, the noise margins represent the maximum amount of noise that can be tolerated on a line feeding the output of a gate to the input of a similar gate. Any noise in excess of this margin will be amplified by more than unity, potentially leading to erroneous circuit behavior. Clearly, the higher the noise margins, the better. In view of the idealized VTC of Fig. 2, the best noise margins are $\mathrm{NM}_L = \mathrm{NM}_H = 0.5V_S$.

VTCs can readily be visualized with a dual-trace oscilloscope operated in the *x-y* mode, or via PSpice. The following code is used to display the VTC of the inverting amplifier of Fig. 4.

```
Displaying a VTC
.lib eval.lib
VS 3 0 dc 5V
vI 1 0 dc 0V
RB 1 2 10k
RC 3 4 1k
Q1 4 2 0 Q2N2222A
.dc vI 0V 5V 100mV
.probe
.end
```

The VTC is shown in Fig. 5. Using simple graphical techniques, one can identify directly on the curve the points where slope is -1 V/V, and hence determine V_{IL} and V_{IH}. Moreover, one can measure V_{OL} and V_{OH}, and thus find the

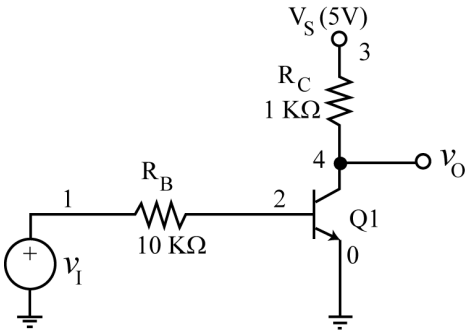


Fig. 4 - Basic inverting amplifier.

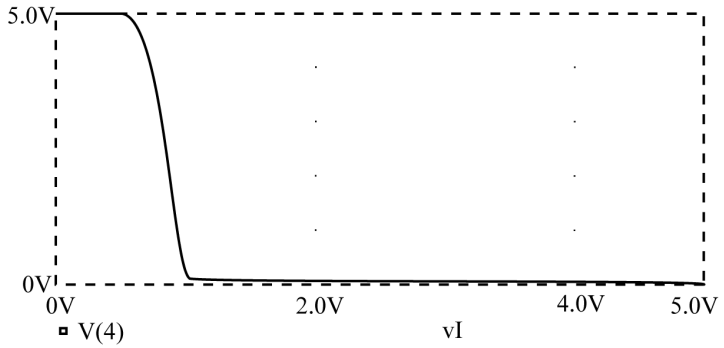


Fig. 5 - VTC of the inverter of Fig. 4.

noise margins.

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, and **S** for SPICE simulation. Moreover, each measured value should be expressed in the form $X \pm \Delta X$ (e.g. $NM_L = 1.3 \pm 0.1$ V), where ΔX represents the estimated uncertainty of your measurement, something you have to figure out based on your learnings in ENGR 300.

BJT Logic Gates:

Shown in Fig. 6 is an inverter of the so called DTL (Diode Transistor Logic) type, a precursor of the more popular TTL (Transistor Transistor Logic) type. As you assemble this and the subsequent circuits, makes sure to keep leads short, and to bypass V_S to ground with a 0.1 μF capacitor. Moreover, any changes to a circuit should be made with power off.

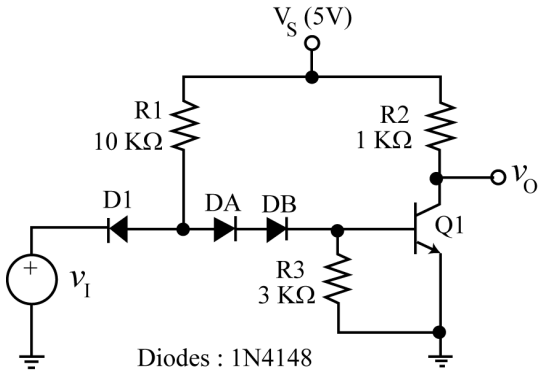
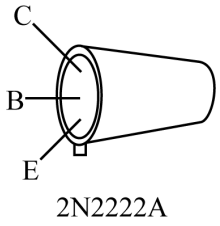


Fig. 6 - DTL inverter.



S1: Using PSpice, along with the built in library models for the 1N4148 diode and the 2N2222A BJT, plot the VTC of the circuit of Fig. 6. Hence, use graphical techniques to determine its noise margins.

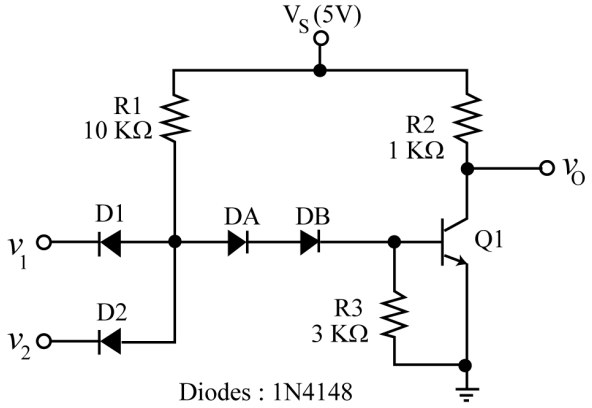
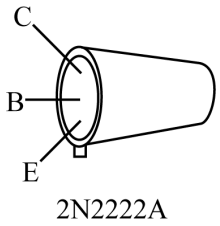


Fig. 7 - Simple DTL logic gate.



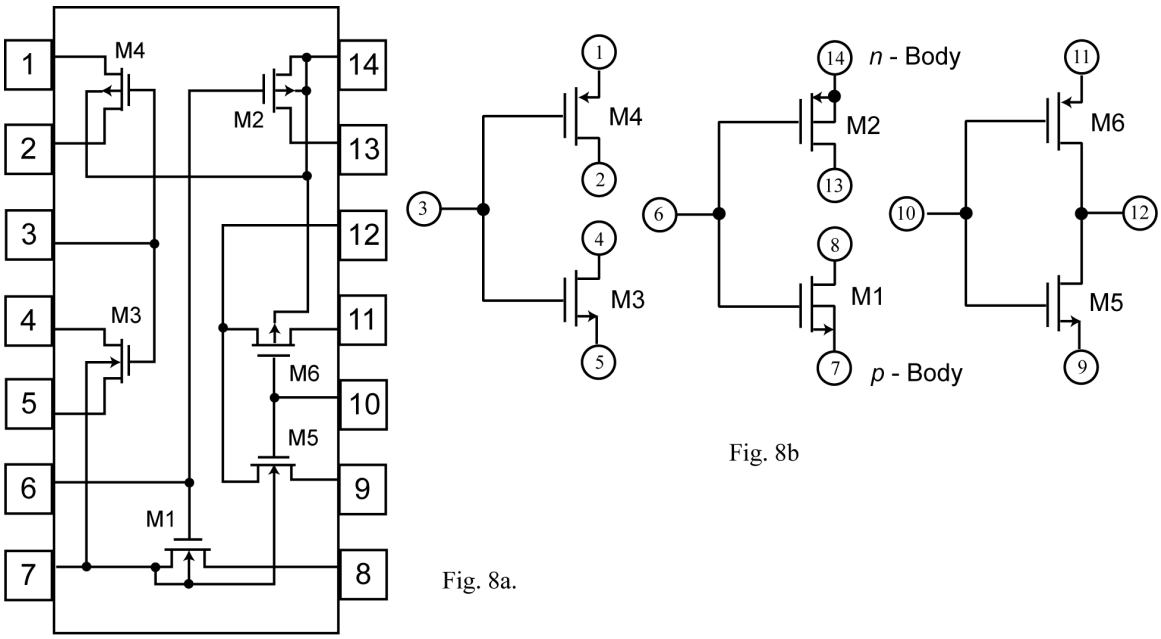


Fig. 8a.

Fig. 8b

Fig. 8 - CD4007 MOSFET array.

MC2: Observe the VTC of the circuit of Fig. 6 experimentally on the oscilloscope, find its noise margins, compare with the values obtained in Step S1 via simulation, and account for possible discrepancies. *Note*: To observe the VTC experimentally, first adjust the signal generator for a triangular wave output of about 100 Hz and alternating between 0 V and 5 V (make your adjustments using Ch. 1 of the oscilloscope, DC Mode, Trigger from Ch. 1). Next, switch the oscilloscope to the *x*-*y* Mode (see ENGR 206), with v_I as the *x* axis (CH. 1, 1 V/div, DC), and v_O as the *y* axis (Ch. 2, 1 V/div, DC). Before connecting the scope to your circuit, adjust the offsets of the two channels so that the origin of the *x*-*y* display (dot) is at the lower left corner of the screen. Also, keep the beam intensity suitably low to avoid burning out the phosphor on the CRT.

MC3: With power off, add diode D_2 as shown in Fig. 7, reapply power, and measure v_O with the DVM for the following input combinations: (v_1, v_2) = (0 V, 0 V), (0 V, 5 V), (5 V, 0 V), (5 V, 5 V). Hence, justify your results in terms of circuit operation. Which of the following logic functions, AND, OR, NAND, NOR, XOR, does your circuit implement? *Note*: for a 0-V input, connect to ground, and for a 5-V input, connect to V_S.

CMOS Logic Gates:

We shall investigate CMOS logic gates using transistors from the CD4007UB MOSFET Array. This array consists of three *n*MOSFETs and three *p*MOSFETs, all of the enhancement type, with the interconnections shown in Fig. 8.

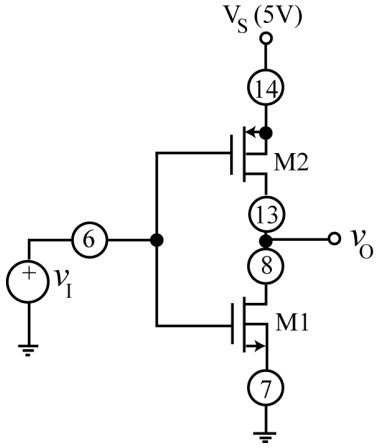


Fig. 9 - Basic CMOS inverter.

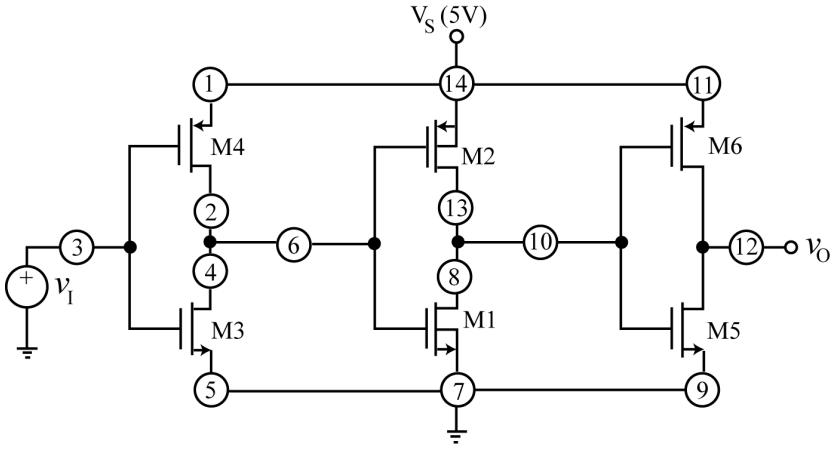


Fig. 10 - Buffered CMOS inverter.

The body of the *n*MOSFETs (pin 7), which is *p*-type, must always be connected to the *most negative voltage* (MNV) in the circuit (ground in the present case), and the body of the *p*MOSFETs (pin 14), which is *n*-type, must always be connected to the *most positive voltage* (MPV) in the circuit (V_S in the present case).

MC4: With power off, connect M_1 and M_2 of your CD4007UB array for inverter operation as in Fig. 9. Hence, reapply power, turn on the signal generator, and repeating the procedure of Step MC2, observe the VTC experimentally on the oscilloscope. Finally, find the noise margins of your inverter.

MC5: With power and the input signal generator off, connect the CD4007UB array to obtain the circuit of Fig. 10, consisting of three inverters connected in cascade, so that the composite circuit still provids logic inversion. Next, reapply power, turn on the signal generator, and observe the VTC experimentally on the oscilloscope. Finally, find the noise margins of this composite inverter, compare with the simple inverter of Fig. 9, and justify its much improved noise margins in terms of circuit operation.

C6: When an odd number n of inverters is connected in ring fashion, as shown in Fig. 11 for the case $n = 3$, the result is a self oscillating circuit called a *ring counter*. Oscillation is due to the nonzero amount of time a signal takes to propagate through a gate, a time aptly called the *gate propagation delay* t_p. For the circuit of Fig. 11, sketch and label the timing diagrams for v_1, v_2, and v_3 for a couple of oscillation cycles, and obtain a relationship between the period of oscillation T and the propagation delay t_p of the gates. *Hint*: Starting with the rising edge of v_1, sketch v_2 and v_3 with each signal delayed by t_p with respect to the preceding one round the ring.

MC7: Disconnect the input signal generator in the circuit of Fig. 10, and connect pins 3 and 12 with a wire to obtain a ring counter. Measure the period T of oscillation with the oscilloscope, and hence use the result of Step C6 to estimate the average propagation delay t_p of each of the three inverters.

M8: With power off, assemble the gate circuit of Fig. 12, consisting of two *n*MOSFETs in *series* and two *p*MOSFETs in *parallel*. Reapply power, and measure v_O with the DVM for the following input combinations: (v_1, v_2) = (0 V, 0 V), (0 V, 5 V), (5 V, 0 V), (5 V, 5 V). Hence, justify your results in terms of circuit operation. Which of the following logic functions, AND, OR, NAND, NOR, XOR, does your circuit implement?

M9: With power off, assemble the gate circuit of Fig. 13, consisting of two *n*MOSFETs in *parallel* and two *p*MOSFETs in *series*. Reapply power, and measure v_O with the DVM for the following input combinations: (v_1, v_2) = (0 V, 0 V), (0 V, 5 V), (5 V, 0 V), (5 V, 5 V). Hence, justify your results in terms of circuit operation. Which of the following logic functions, AND, OR, NAND, NOR, XOR, does your circuit implement?

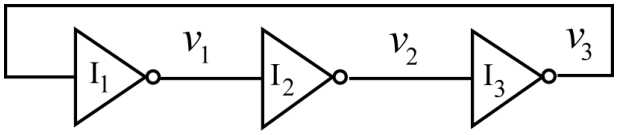


Fig. 11 - Ring counter.

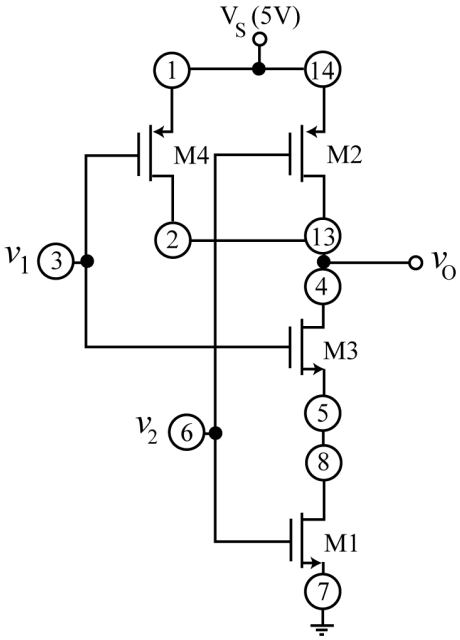


Fig. 12 – Basic CMOS logic gate.

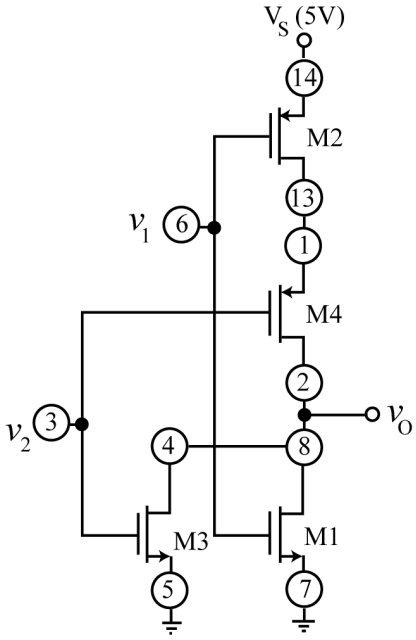


Fig. 13 – Basic CMOS logic gate.