ENGR 301 – Electrical Measurements

Experiment # 5: MOSFET Characteristics and Applications

Objective:
To characterize *n-channel* and *p-channel enhancement MOSFETS*. To investigate basic *MOSFET amplifiers*. To compare *measured* and *simulated* MOSFET circuits.

Components:
2 × CD4007UB MOSFET Arrays, 2 × 0.1 μF capacitors, 1 × 10 kΩ potentiometer, and miscellaneous resistors:
1 × 100 Ω, 4 × 10 kΩ, and 1 × 1 MΩ (all 1%, ¼ W).

Instrumentation:
A bench power supply, a signal generator (sine/triangle wave), a digital multimeter, and a dual-trace oscilloscope.

References:

1. Sedra, Adel S., and Smith, Kenneth C., *Microelectronics*, 4th Ed, Oxford University Press, 1997.
2. Roberts, Gordon W., and Sedra, Adel S., *SPICE*, 2nd Ed., Oxford University Press, 1997.

Theoretical Background:
When an *n*-channel MOSFET (*n*MOSFET) is biased in the *active region*, also called *pinchoff* or *saturation region*, and defined by the conditions

$$v_{GS} \geq V_{tn} \quad (1a)$$
$$v_{DS} \geq v_{GS} - V_{tn} \quad (1b)$$

its drain current i_D is related to the applied gate-source voltage v_{GS} and the operating drain-source voltage v_{DS} as

$$i_D = (k_n/2) \times (v_{GS} - V_{tn})^2 \times (1 + \lambda_n v_{DS}) \quad (2)$$

where k_n, a scale factor whose units are A/V^2, is called the *device transconductance parameter*; V_{tn} is called the *threshold voltage*; and λ_n, whose dimensions are V^{-1}, is called the *channel length modulation parameter* (λ_n is the reciprocal of the Early voltage V_A of BJTs, or $\lambda_n = 1/V_{An}$). For low power MOSFETs, k_n is typically in the range of 10^1 to 10^2 μA/V^2, V_{tn} is in the range of a few V, and λ_n is on the order of 10^{-1} to 10^{-2} V^{-1}. A given pair of values I_D and V_{DS} in the i_D-v_{DS} plane define a unique point called the *operating point* $Q(I_D, V_{DS})$ of the MOSFET.

The device transconductance parameter k_n depends on device geometry as

$$k_n = k'\left(\frac{W_n}{L_n}\right) \quad (3)$$

where *k'*, also in A/V^2, is called the *process transconductance parameter*; and W_n and L_n, both in μm, are the channel *width* and channel *length* of the MOSFET.

If $V_{tn} > 0$, the *n*MOSFET is said to be of the *enhancement type*; if $V_{tn} < 0$, it is said to be of the *depletion type*. The threshold voltage V_{tn} depends on the body bias voltage V_{SB} as

$$V_{tn} = V_{tn0} + \gamma_n\left(\sqrt{2\phi_{fn} + V_{SB}} - \sqrt{2\phi_{fn}}\right) \quad (4)$$

where V_{tn0} is the threshold voltage in the absence of any body bias ($V_{SB} = 0$); γ_n, in V$^{1/2}$, is called the *body effect coefficient*, and is typically 0.5 V$^{1/2}$; finally, ϕ_{fn} is the *equilibrium electrostatic potential* of the body, typically 0.3 V.

Note that for *n*MOSFETs the *body*, or *substrate*, must *never* be biased *more positive* than the source, that is, we must always have $V_{SB} \geq 0$.

Similar considerations hold for *p*-channel MOSFETs (*p*MOSFETs), provided we *reverse* all current directions and voltage polarities. Thus, while in an *n*MOSFET i_D flows *into* and i_S flows *out* of the device, in a *p*MOSFET i_D flows *out* and i_S flows *into* the device. Moreover, the active region conditions of Eq. (1) become, for a *p*MOSFET,

$$v_{SG} \geq -V_{tp} \qquad (5a)$$

$$v_{SD} \geq v_{SG} + V_{tp} \qquad (5b)$$

Similarly, Eq. (2) is rephrased as

$$i_D = \left(\frac{k_p}{2}\right) \times \left(v_{SG} + V_{tp}\right)^2 \times \left(1 + \lambda_p v_{SD}\right) \qquad (6)$$

where $k_p = k'(W_p/L_p)$ is the device transconductance parameter. If $V_{tp} < 0$, the *p*MOSFET is said to be of the *enhancement type*; if $V_{tp} > 0$, it is said to be of the *depletion type*. Equation (3) holds for all MOSFETs, regardless of the channel type, while Eq. (4) becomes, for a *p*MOSFET,

$$V_{tp} = V_{tp0} - \gamma_p \left(\sqrt{-2\phi_{fp} + V_{BS}} - \sqrt{-2\phi_{fp}}\right) \qquad (7)$$

Where now ϕ_{fp} is typically -0.3 V. Note that for *p*MOSFETs the *body*, or *substrate*, must *never* be biased *more negative* than the source, that is, we must always have $V_{BS} \geq 0$.

MOSFET circuits are readily simulated using PSpice. To this end, we must first create a MOSFET model which, for the case of an *n*-channel device called `our_nMOSFET` takes on the form

```
.model our_nMOSFET nmos (kp=kval Vto=Vval lambda=lval gamma=gval)
```

where `kval`, `Vval`, `lval`, and `gval` are, respectively, the measured values of k', V_{tn0}, λ_n, and γ_n.
Then, to invoke a transistor `MXXX`, we use a statement of the type

```
MXXX D G S B our_nMOSFET W=Wval L=Lval
```

where `D`, `G`, `S`, and `B` are the drain, gate, source, and body terminals, in that specific order, and `Wval` and `Lval` are the values of W_n and L_n. The following PSpice code uses the circuit of Fig. 1 to display the i_D-v_{DS} characteristics of an enhancement *n*MOSFET called `M1` and having $W_n = L_n = 10$ µm, $k' = 200$ µA/V^2, $V_{tn0} = 1.5$V, and $\lambda_n = 0.05$ V^{-1}:

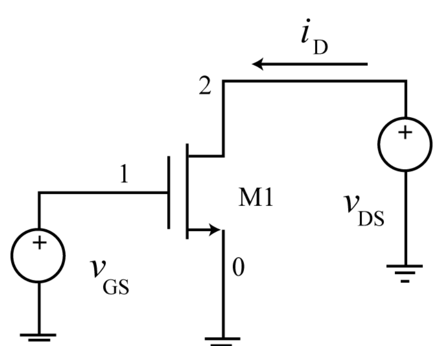

Fig. 1 - PSpice circuit to display the *i*-*v* characteristics of a MOSFET.

```
MOSFET Characteristics
vGS 1 0 dc 0V
vDS 2 0 dc 0V
M1 2 1 0 0 our_nMOSFET W=10u L=10u
.model our_nMOSFET nmos (kp=200u Vto=1.5V lambda=0.05)
.dc vDS 0V 10V 100mV vGS 0V 5V 0.5V
.probe
.end
```

The characteristics are shown in Fig. 2.

The following PSpice code is used to simulate the basic CS amplifier of Fig. 3 using the same MOSFET model of above:

```
CS Amplifier
VDD 3 0 dc 10V
vs 1 0 ac 100mV
C1 1 2 0.1uF
RG 2 4 10Meg
RD 3 4 10k
M1 4 2 0 0 our_nMOSFET W=10u L=10u
.model our_nMOSFET nmos (kp=200u Vto=1.5V lambda=0.05)
C2 4 5 1uF
RL 5 0 100k
.ac lin 1 10kHz 10kHz
.print ac Vm(1) Vp(1) Vm(5) Vp(5)
.end
```

After running PSpice, we obtain an output file with the following information:

```
BIAS SOLUTION:
NODE     VOLTAGE     NODE     VOLTAGE     NODE     VOLTAGE
(1)       0.0000     (2)       3.7858     (3)      10.0000
NODE     VOLTAGE     NODE     VOLTAGE
(4)       3.7858     (5)       0.0000

AC ANALYSIS:
 FREQ   VM(1)   VP(1)   VM(5)   VP(5)   1.000E+04   1.000E+00   0.000E+00   3.991E-0100   -1.800E+02
```

We readily find the gain of this amplifier to be v_o/v_s = VM(5)/VM(1) = -0.3991/0.1 = -3.991 V/V, where the negative sign is implied by the fact that VP(5) = -180°. You may find it instructive to confirm the above data (both bias and ac) via hand calculations!

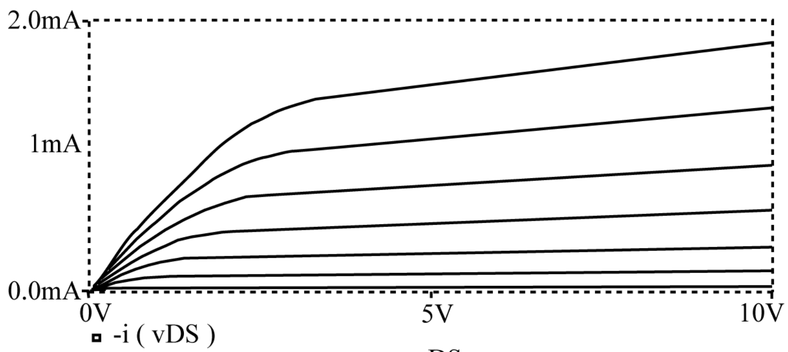

Fig. 2 - PSpice plot for the MOSFET of Fig. 1.

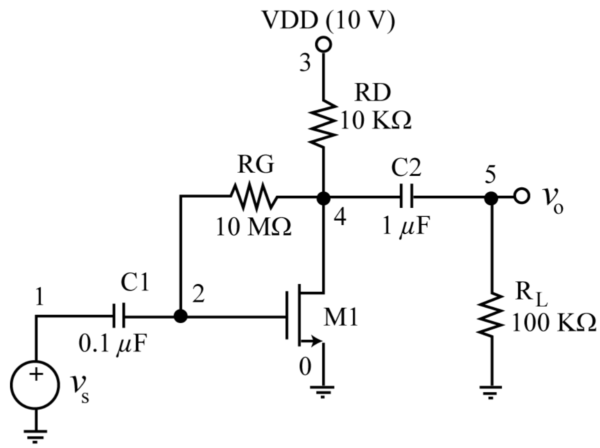

Fig. 3 - Simple MOSFET amplifier.

The CD4007UB MOSFET Array:

We shall perform our measurements and experiments using the CD4007UB MOSFET Array. This array consists of three *n*MOSFETs and three *p*MOSFETs, all of the enhancement type, with the interconnections shown in Fig. 4. Note that the body of the *n*MOSFETs (pin 7), which is *p*-type, must always be connected to the *most negative voltage* (MNV) in the circuit; likewise, the body of the *p*MOSFETs (pin 14), which is *n*-type, must always be connected to the *most positive voltage* (MPV) in the circuit. Failure to respect these constraints may invalidate all measurements taken.

Pinchoff-Region Characteristics:

We shall use the circuits of Figs. 5 and 6 to find V_t and k, the circuits of Figs. 7 and 8 to find λ, and the circuits of Figs.9 and 10 to find γ. In the circuits of Figs. 5 and 6 v_S is a variable DC source which is used along with R to establish prescribed values of i. To perform your i and v measurements, first configure your digital multimeter (DMM) as an *ammeter in series* between the resistance R and the drain D to set i, then as a *voltmeter in parallel* with the MOSFET to measure v. In case your ammeter has been put it out of service by abuse, you can still use your DMM to perform current measurements as follows: Before inserting R in the circuit, measure it with the ohmeter; then insert R, and while monitoring with the voltmeter the voltage v_R across R, adjust v_S for the desired value of i (for instance, to obtain i = 100 μA with R = 98 kΩ, adjust v_S until $v_R = R \times i = 98 \times 0.100 = 9.8$ V).

Fig. 4 - CD4007 MOSFET Array.

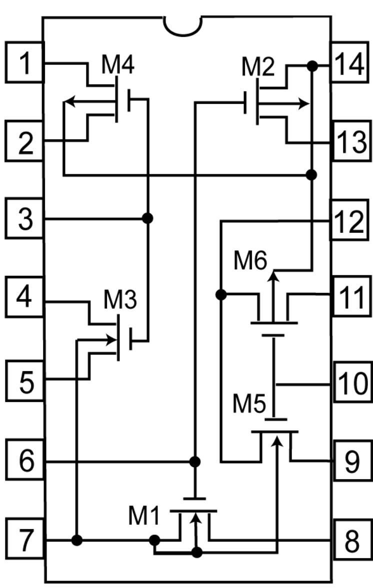

Fig. 4 (a)

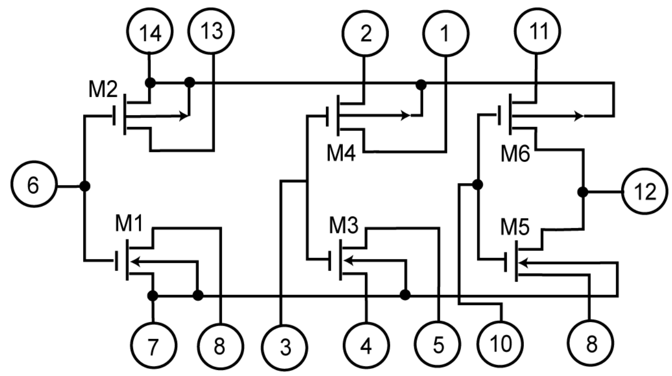

Fig. 4 (b)

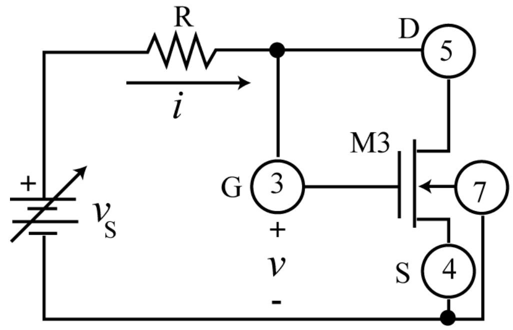

Fig. 5 - Circuit setup to characterze a *n*MOSFET.

Mark one of your CD4007UB ICs, and as you interconnect parts of it in the circuits below, use short leads and bypass the power supplies with 0.1-μF capacitors, as recommended in Appendix A2.

M1: For the *n*MOSFET of Fig. 5, measure v for the following values of i (shown within parentheses are the corresponding recommended values of R): i = 0.1 mA (100 kΩ), i = 0.4 mA (20 kΩ; use 2 × 10-kΩ resistors in series), and i = 2 mA (5.0 kΩ; use 2 × 10-kΩ resistors in parallel). Then, repeat for the *p*MOSFET of Fig. 6. As usual, all your data should be expressed in the form $X \pm \Delta X$.

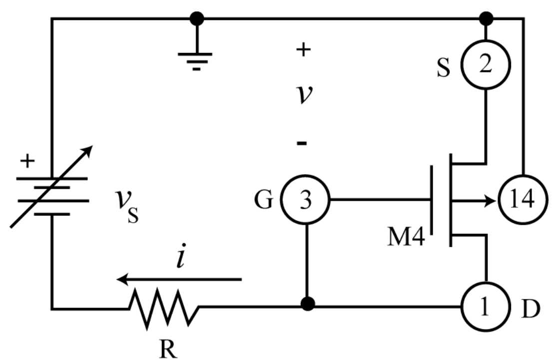

Fig. 6 - Circuit setup to characterize a *p*MOSFET.

M2: For the *n*MOSFET of Fig. 7 adjust the potentiometer until V_{DS} = 5 V (for R_D use 2 × 10-kΩ resistors in parallel). Also, record the value of V_{GS}, which will be needed in Step M6. Next, turn off power, configure your DMM as a DC ammeter, break the circuit at node *D*, insert the ammeter in series, reapply power and measure I_D both with R_D in place as shown, and with R_D shorted out with a wire. The difference ΔI_D between the two readings will be small, so make sure to use as many digits as your ammeter will allow. Note that shorting out R_D is designed to cause a change ΔV_{DS} = 5 V. As usual, all your data should be expressed in the form $X \pm \Delta X$.

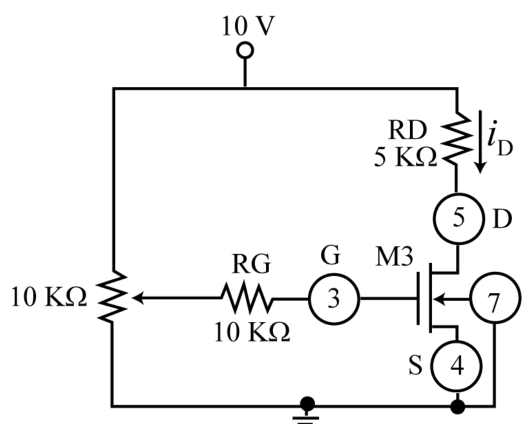

Fig. 7 - Circuit to determine λ_n.

M3: Repeat Step M2 for the *p*MOSFET of Fig. 8, after having adjusted the potentiometer for $V_{SD} = 5$ V. Record also the value of V_{SG}, which will be needed in Step M7.

C4: Using the *n*MOSFET data of Step M2, find $r_{on} = \Delta V_{DS}/\Delta I_D$ and, hence, $\lambda_n = 1/V_{An} = 1/(r_{on}I_D - V_{DS})$. Likewise, using the *p*MOSFET data of Step M3, find $r_{op} = \Delta V_{SD}/\Delta I_D$ and, hence, $\lambda_p = 1/V_{Ap} = 1/(r_{op}I_D - V_{SD})$.

C5: Let us now introduce the quantities

$$x = v \qquad y = \sqrt{\frac{i}{1+\lambda v}}$$

Using the *n*MOSFET set of i and v data of Step M1, along with the value of λ_n found in Step C4, calculate the corresponding values of y, plot them on x-y graph paper, and draw the best fit straight line; in view of Eq. 2, the intercept of this line with the x-axis yields V_{tn0}, and its slope yields $(k_n/2)^{1/2}$, which allows us in turn to find k_n. Then repeat the procedure for the *p*MOSFET, keeping in mind that in this case the intercept of the best fit straight line with the x-axis yields $-V_{tp0}$, and its slope yelds $(k_p/2)^{1/2}$, which, in turn, we use to find k_p.

MC6: Turn power off in the circuit of Fig. 7, lift the *p*-body (pin 7) off ground, and return it to a –5-V supply via a protective 10-kΩ series resistor as shown in Fig. 9. Reapply power, adjust the potentiometer until you get again $V_{DS} = 5$ V, and record the new value of V_{GS}. Then, apply Eq. (4) to find

$$\gamma_n = \frac{\Delta V_{GS}}{\sqrt{2\phi_{fn} + V_{SB}} - \sqrt{2\phi_{fn}}}$$

where ΔV_{GS} is the difference between the current value of V_{GS} and that found in Step M2, and $\phi_{fn} = 0.3$ V.

MC7: Turn power off in the circuit of Fig. 9, lift the *n*-body (pin 14) off ground, and return it to a +5-V supply via a protective 10-kΩ series resistor as shown in Fig. 10. Reapply power, adjust the potentiometer until you get again $V_{SD} = 5$ V, and record the new value of V_{SG}. Then, apply Eq. (7) to find

$$\gamma_p = \frac{\Delta V_{SG}}{\sqrt{-2\phi_{fp} + V_{BS}} - \sqrt{-2\phi_{fp}}}$$

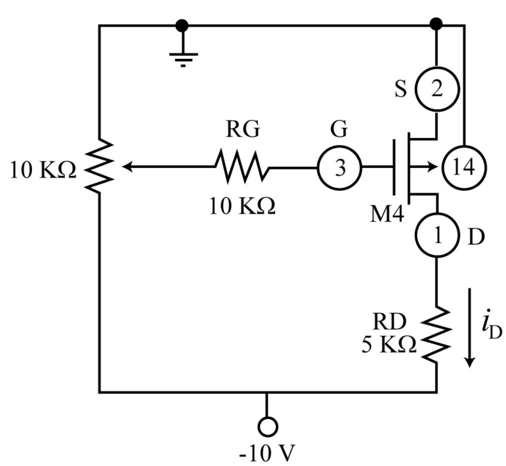

Fig. 8 - Circuit to determine λ_p.

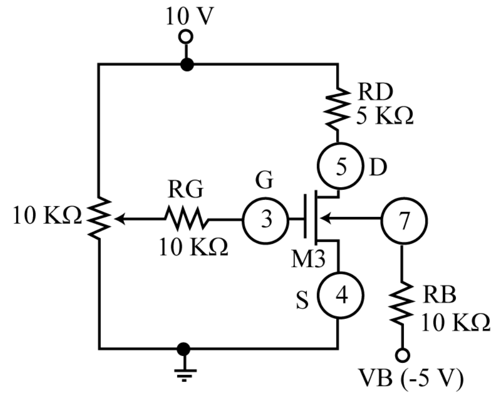

Fig. 9 - Circuit to determine γ_n.

where ΔV_{SG} is the the difference between the current value of V_{SG} and that recording Step M3, and $\phi_{fn} = -0.3$ V. Summarize your numerical findings for k_n, V_{tn0}, λ_n, γ_n, and k_p, V_{tp0}, λ_p, γ_p, and express all data in the form $X \pm \Delta X$.

S8: Use PSpice to display the i_D-v_{DS} characteristics of your *n*MOSFET, as well as the i_D-v_{SD} characteristics of your *p*MOSFET. Do it both for the case of 0-V and 5-V body bias. Comment on your findings.

Common-Source Amplifier:

With power off, assemble the circuit of Fig. 11, keeping the leads short and bypassing the power supply with a 0.1 µF capacitor.

C9: Predict the DC voltage V_D at the drain terminal in Fig. 11, as well as the small signal gain $A_v = v_o/v_s$.

M10: While monitoring v_s with Ch.1 of the oscilloscope (DC mode, Trigger on Ch. 1), adjust the signal generator so that v_s in Fig. 11 is a 10-kHz sinewave with 0-V DC and 0.5-V peak amplitude. Next, use CH. 2 (DC mode, Chop Mode), to measure the DC voltage at the drain pin; finally, switch Ch. 2 to the AC mode and measure the peak amplitude of v_o; hence, find the gain $A_v = v_o/v_s$ of your amplifier.

S11: Simulate the circuit of Fig. 11 using PSpice. For a realistic simulation, you need to create a PSpice model for your specific *n*MOSFET sample, using the above measured values of k_n, V_{tn0}, λ_n, and γ_n.

C12: Compare the predicted values of Step C9 with the measured values of Step M10 and the simulated values of Step S11; account for any possible discrepancies.

M13: Returning to the circuit of Fig. 11, switch Ch. 2 back to the DC mode (make sure you know where your 0-V baseline is on the screen!), change the input generator's waveform to triangular, and rise its amplitude until v_o distorts both at the top and at the bottom. Justify the two types of distortion in terms of transistor operation.

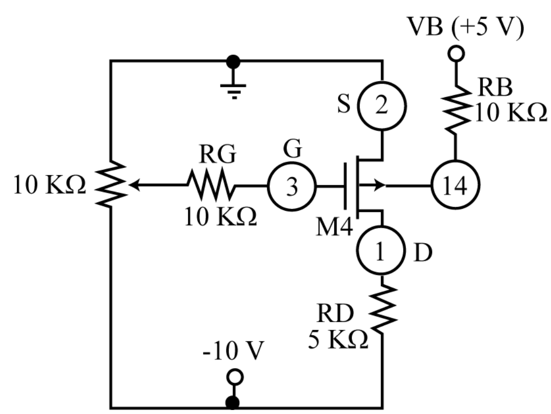

Fig. 10 - Circuit to determine γ_p.

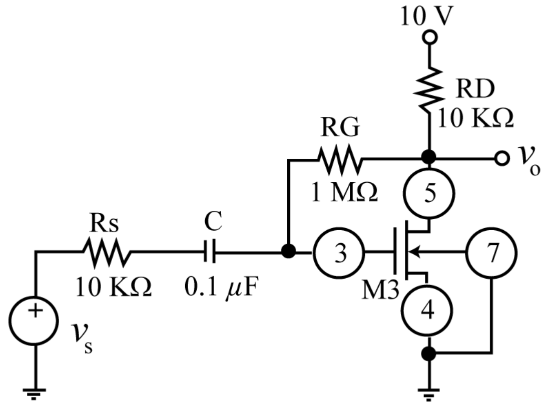

Fig. 11 - Common-source amplifier.

Common-Drain Amplifier:

With power off, assemble the circuit of Fig. 12, keeping leads short and using a 0.1-μF power supply bypass capacitor, as usual. Then, adjust the input source so that v_s is a 10-kHz sinewave with 0-V DC and 2-V of peak-to-peak amplitude.

CMS14: In Fig. 12 predict the DC voltage V_S, as well the small signal gain $A_v = v_o/v_i$. Next, measure V_S and A_v. Next, find V_S and A_v via PSpice. Finally, compare the three sets of values, and account for possible discrepancies.

CMOS Amplifier:

One of the most popular MOSFET amplifier configurations is the *complementary MOS* (CMOS) cell of Fig. 13, consisting of an *n*MOSFET and a *p*MOSFET with the gates tied together to form the input node, and the drains tied together to form the output node. As you assemble this circuit, keep leads short and use a 0.1-μF power supply bypass capacitor, as usual. Since this stage exhibits a fairly high gain, its input v_i must be suitably small, so we interpose a voltage divider R_1 and R_2 between the input source and the amplifier to suitably scale down the source. With the resistances shown we have $v_i \cong v_s/100$.

C15: For the circuit of Fig. 13 predict the DC output voltage V_O as well as the small signal gain $A_v = v_o/v_i$.

M16: While monitoring v_s with Ch.1 of the oscilloscope (DC mode, Trigger from Ch. 1), adjust the input signal generator so that v_s in Fig. 13 is a 10-kHz sinewave with 0-V DC and 1-V peak amplitude (this makes v_i a 10-mV peak amplitude sinewave). Next, use CH. 2 (DC mode, Chop Mode), to measure V_O. Now, switch Ch. 2 to the AC mode and measure the peak amplitude of v_o; finally, find the gain $A_v = v_o/v_i$ of your amplifier.

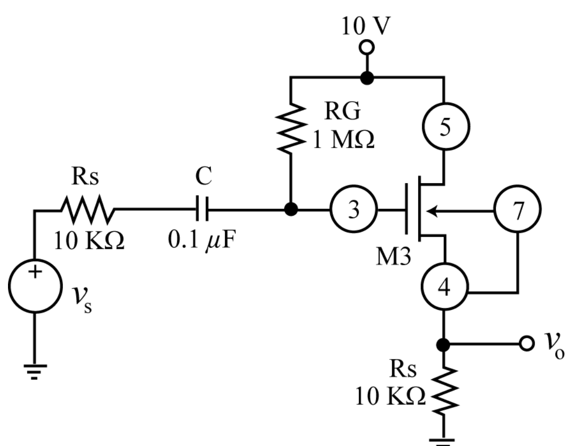

Fig. 12 - Common-drain amplifier.

SC17: Simulate the circuit of Fig. 13 using PSpice; then, compare predicted, measured, and simulated values, and account for any possible discrepancies.

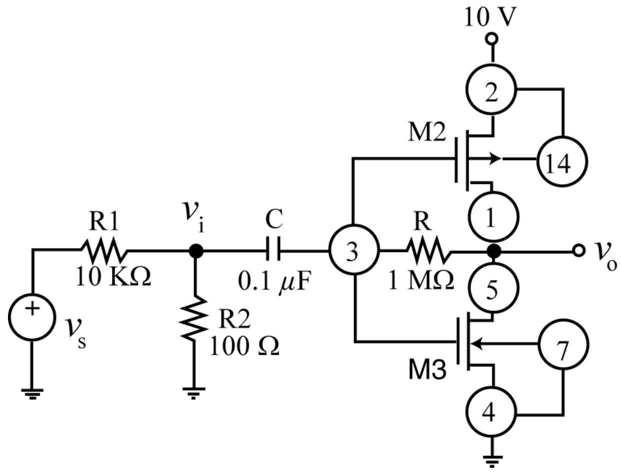

Fig. 13 – CMOS amplifier.