ENGR 301 – Electrical Measurements

Experiment # 4: BJT Characteristics and Applications

Objective:

To characterize a *bipolar junction transistor* (BJT). To investigate basic BJT *amplifiers* and *current sources*. To compare *measured* and *simulated* BJT circuits.

Components:

2 × 2N2222A *npn* BJTs, 2 × 2N3906 *pnp* BJTs, 1 × 1N4733 5.1 V, 1 W zener diode, 2 × 0.1 μF capacitors, 1 × 100 μF capacitor, 1 × 10 kΩ potentiometer, and miscellaneous resistors: 1 × 100 Ω, 1 × 1.0 kΩ, 1 × 2.0 kΩ, 1 × 3.0 kΩ, 4 × 10 kΩ, and 1 × 100 kΩ (all 1%, ¼ W).

Instrumentation:

A curve tracer, a bench power supply, a signal generator (sine/triangle wave), a digital multimeter, and a dual-trace oscilloscope.

References:

1. Sedra, Adel S., and Smith, Kenneth C., *Microelectronics*, 4th Ed, Oxford University Press, 1997.
2. Roberts, Gordon W., and Sedra, Adel S., *SPICE*, 2nd Ed., Oxford University Press, 1997.

Theoretical Background:

When a low-power *npn* BJT is biased in the *forward-active region*, defined by by the conditions

$$v_{BE} = V_{BE(\text{on})} \quad (1a)$$
$$v_{CE} \geq V_{CE(\text{sat})} \quad (1b)$$

its collector current i_C is related to the applied base-emitter voltage drop v_{BE} and the operating collector-emitter voltage v_{CE} as

$$i_C = I_S e^{v_{BE}/V_T} \times \left(1 + \frac{v_{CE}}{V_A}\right) \quad (2)$$

where I_S , a current scale factor, is called the *collector saturation current*; V_T, a voltage scale factor, is called the *thermal voltage*; V_A, another voltage scale factor, is called the *Early voltage*. At room temperature, $V_T \cong 26$ mV and I_S is typically on the order of fAs for a low-power BJT. Moreover, a low-power *npn* BJT typically exhibits $V_{BE(\text{on})} \cong 0.7$ V and $V_{CE(\text{sat})} \cong 0.1$ V; finally, V_A is on the order of 10^2 V. Note that the extrapolated value of i_C in the limit $v_{CE} \rightarrow 0$ is $i_C = I_S$ [exp (v_{BE} /V_T)]. A given pair of values I_C and V_{CE} in the i_C-v_{CE} plane define a unique point called the *operating point* $Q(I_C, V_{CE})$ of the BJT.

Similar considerations hold for *pnp* BJTs, provided we *reverse* all current directions and voltage polarities. Thus, while in an *npn* BJT i_C and i_B flow *into* and i_E flows *out* of the device, in a *pnp* BJT i_C and i_B flow *out* of and i_E flows *into* the device. Moreover, the forward-active conditions of Eq. (1) become, for a *pnp* BJT,

$$v_{EB} = V_{EB(\text{on})} \cong 0.7 \text{ V} \quad (3a)$$
$$v_{EC} \geq V_{EC(\text{sat})} \cong 0.1 \text{ V} \quad (3b)$$

Similarly, Eq. (2) is rephrased as

$$i_C = I_S e^{v_{EB}/V_T} \times \left(1 + \frac{v_{EC}}{V_A}\right) \quad (4)$$

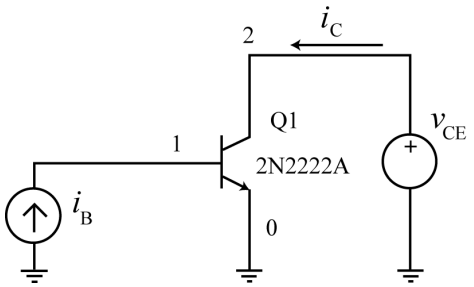


Fig. 1 – PSpice circuit to investigate the *i-v* characteristics of a BJT.

The terminal currents of a forward-biased *npn* and *pnp* BJT are related as

$$i_C = \alpha_F i_E = \beta_F i_B \qquad i_B = i_C/\beta_F = i_E/(\beta_F + 1) \qquad i_E = i_C/\alpha_F = (\beta_F + 1)i_B \qquad (5)$$

where

$$\beta_F = \alpha_F/(1 - \alpha_F) \qquad \alpha_F = \beta_F/(\beta_F + 1) \qquad (6)$$

Typically, α_F is very close to unity (e.g. $\alpha_F = 0.99$), and β_F is on the order of 10^2.

BJT circuits are readily simulated using PSpice. The file `Eval.lib` that comes with the student version of PSpice contains models for popular BJTs, including the 2N2222A *npn* and the 2N3906 *pnp* BJT. For instance, to invoke a 2N2222A BJT from the built in library, we use a command of the type

```
QXXX C B E Q2N2222A
```

where `QXXX` is the name of the specific BJT, such as `Q1`, and `C`, `B`, and `E` are the collector, base, and emitter nodes, in that specific order. Shown below is the PSpice code for the curve tracer circuit of Fig. 1, which is used to display the i_C -v_{CE} characteristics of a 2N2222A BJT called `Q1`:

```
BJT Characteristics
.lib eval.lib
iB 0 1 dc 0uA
vCE 2 0 dc 0V
Q1 2 1 0 Q2N2222A
.dc vCE 0V 10V 100mV iB 0uA 10uA 1uA
.probe
.end
```

The characteristics are shown in Fig. 2.

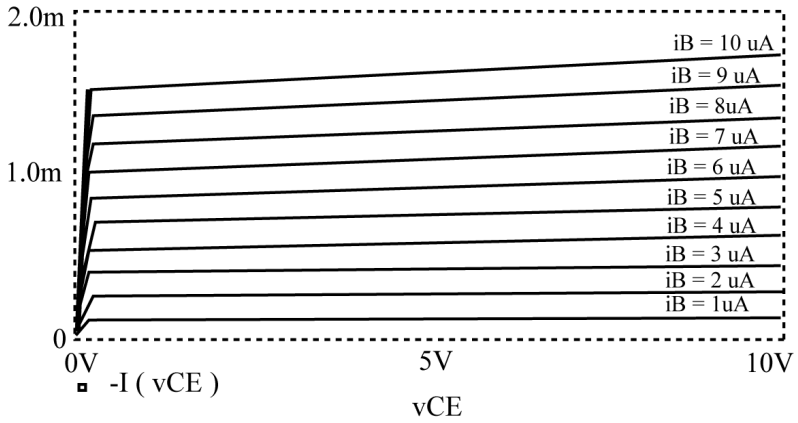


Fig. 2 - *i-v* characteristics of a BJT.

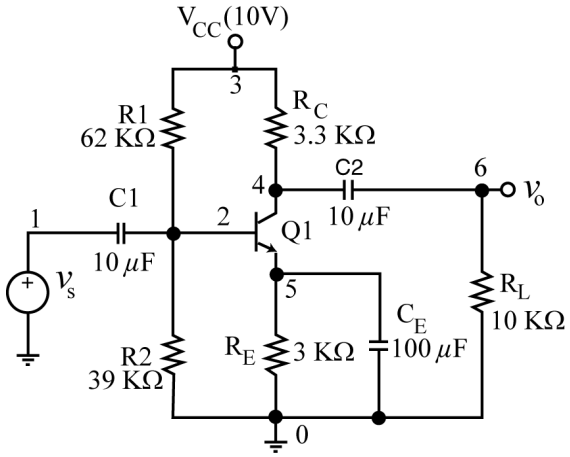


Fig. 3 - Basic CE amplifier.

The following PSpice code is used to simulate the basic CE amplifier of Fig. 3:

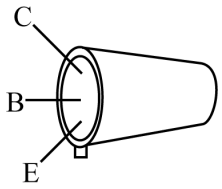
```
CE Amplifier
.lib eval.lib
VCC 3 0 dc 10V
vs 1 0 ac 10mV
C1 1 2 10uF
R1 3 2 62k
R2 2 0 39k
RC 3 4 3.3k
RE 5 0 3.0k
CE 5 0 100uF
Q1 4 2 5 Q2N2222A
C2 4 6 10uF
RL 6 0 10k
.ac lin 1 10kHz 10kHz
.print ac Vm(1) Vp(1) Vm(6) Vp(6)
.end
```

After running PSpice, we obtain an output file with the following information:

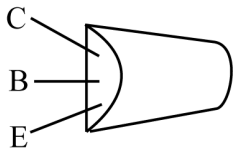
```
BIAS SOLUTION:

NODE    VOLTAGE    NODE    VOLTAGE    NODE    VOLTAGE
(1)      0.0000    (2)      3.7032    (3)     10.0000
NODE    VOLTAGE    NODE    VOLTAGE    NODE    VOLTAGE
(4)      6.6580    (5)      3.0580    (6)      0.0000

AC ANALYSIS:

  FREQ         VM(1)        VP(1)        VM(6)        VP(6)
1.000E-02   0.000E+00   9.351E-01  -1.797E+02   1.000E+04
```

We readily find the gain of this amplifier to be v_o/v_s = `VM(6)/VM(1)` = -93.51 V/V, = -0.9351/0.01 where the negative sign is implied by the fact that `VP(6)` ≅ -180°. You may find it instructive to confirm the above data (both bias and ac) via hand calculations!

BJT Pinouts



2N2222A



2N3906

Curve Tracers:

The i_C -v_{CE} characteristics of BJTs can be displayed experimentally on a cathode ray tube (CRT) by means of an instrument called *curve tracer*. An example of such an instrument is the Tektronix Type 575 Transistor Curve Tracer available in our lab. Use the following steps to calibrate the instrument for displaying the i_C -v_{CE} characteristics of a 2N2222A *npn* BJT:

1. Locate the VERTICAL and HORIZONTAL selectors, in the upper right area of the front panel, and set them, respectively, to 0.1 mA /div and 1 V/div; adjust the POSITION knobs immediately below so that the origin of the *i*-*v* characteristic is at the lower left corner of the CRT.

2. Locate the BASE STEP GENERATOR controls, in the lower right area of the front panel; set the selector switch to REPETITIVE; turn the STEPS/FAMILY knob fully clockwise; set the POLARITY knob to +; set the SERIES RESISTOR selector to 22 kΩ; set the STEP SELECTOR to 0.02 mA.

3. Locate the COLLECTOR SWEEP controls, in the lower left area of the front panel; set the PEAK VOLTAGE RANGE knob to 0-20 A; set the POLARITY knob to +; set the PEAK VOLTS RANGE selector to 40 V; set the DISSIPATION LIMITING RESISTOR selector to 10 kΩ.

4. Locate the small horizontal panel at the very bottom; set the TRANSISTOR A or B selector switch to the neutral position; insert the BJT to be tested into one of the two sockets, say TRANSISTOR B, making sure its C, B, and E leads match those of the socket; set the selector switch to TRANSISTOR B, and observe the *i*-*v* characteristics on the CRT. Fiddle around with the knobs a bit, as needed for optimal visualization and measurements.

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, and **S** for SPICE simulation. Moreover, each measured value should be expressed in the form $X \pm \Delta X$ (e.g. $\beta_F = 125 \pm 1$), where ΔX represents the estimated uncertainty of your measurement, something you have to figure out based on your learnings in ENGR 300.

Forward-Active Characteristics:

The PSpice model used in the above examples is based on *typical* 2N2222A parameter values as reported in the data sheets. An actual BJT sample exhibits its own set of parameters, and we will measure some of them to gain an idea of its departure from typical data.

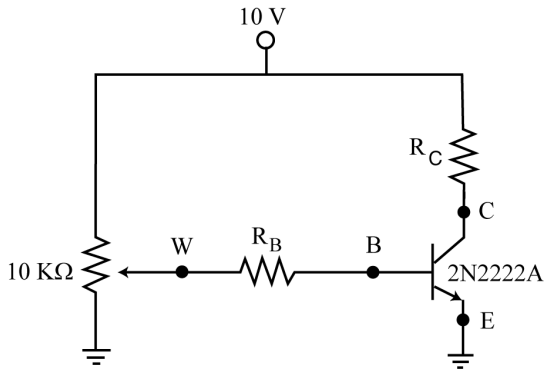


Fig. 4-Circuit to investigate the FA characteristics.

M1: Mark one of your 2N2222A BJTs, and use the curve tracer to measure β_F and r_o at the operating point $Q(I_C, V_{CE}) = Q(1\text{ mA}, 5\text{ V})$. Recall that $\beta_F = I_C/I_B$, where I_B is the base current required to sustain the desired I_C, and that $1/r_o$ is the slope of the i_C-v_{CE} curve at Q. Then, estimate the Early voltage V_A from $1/r_o = I_C/(V_A + V_{CE})$. Don't forget to express your data in the form $X \pm \Delta X$. *Note*: If the curve tracer is already in use by another group, proceed with the next steps and return to the present one later.

M2: With power off, assemble the circuit of Fig. 4 with $R_C = 5.0\text{ k}\Omega$ (use $2 \times 10\text{-k}\Omega$ resistors in parallel) and $R_B = 500\text{ k}\Omega$ (use $2 \times 1.0\text{-M}\Omega$ resistors in parallel); keep the leads short, and bypass the power supply bus with a 0.1-μF capacitor, as recommended in Appendix A2. Then, apply power and adjust the potentiometer until $V_{CE} \cong 5\text{ V}$; record also the voltages V_W and V_{BE} (when measuring V_{BE}, use as many digits as your DVM will allow).

M3: Turn power off, configure your DMM as a DC ammeter, break the circuit at node C, and insert the ammeter in series; then, reapply power and measure I_C both with R_C in place, as shown, and with R_C shorted out with a wire. The difference ΔI_C between the two readings will be small, so make sure you use as many digits as your ammeter will allow. Note that shorting out R_C is designed to cause a change $\Delta V_{CE} = 5\text{ V}$.

C4: Use the data of Steps M2 and M3 to compute β_F, V_A, and I_S at the operating point $Q(1\text{ mA}, 5\text{ V})$ as follows:

(a) $\beta_F = I_C/I_B$, where I_B is found as $I_B = (V_W - V_{BE})/R_B$. You may want to measure also R_B for more accurate results (don't forget to pull R_B out of the circuit when measuring it!)

(b) $V_A = r_o I_C - V_{CE}$, where $r_o = \Delta V_{CE}/\Delta I_C$

(c) $I_S = \dfrac{I_C}{e^{V_{BE}/V_T} \times \left(1 + V_{CE}/V_A\right)}$, where you are to assume $V_T = 26\text{ mV}$

Don't forget to express your data in the form $X \pm \Delta X$. Then, compare the values of β_F and V_A with those of Step M1, and comment. Which set of values do you think is more dependable?

Saturation Characteristics:

To observe these characteristics we use again the circuit of Fig. 4, but with $R_C = 10\text{ k}\Omega$ and $R_B = 100\text{ k}\Omega$. As you make these changes, don't forget to turn power off!

M5: Starting with the wiper voltage v_W at zero, gradually rise v_W while monitoring v_{CE} with the DVM. As v_W rises, v_{CE} decreases until it saturates at $v_{CE} = V_{CE(sat)}$. Record the values of v_W, v_{BE}, and v_{CE} at the point when v_{CE} just begins to saturate, a situation aptly referred to as the *edge-of-saturation*. Use the above data to calculate the ratio I_C/I_B at the edge of saturation; how does this ratio compare with the value of β_F found earlier?

M6: Now rise the wiper all the way up to 10 V, while still monitoring v_{CE} with the DVM. Does v_{CE} change appreciably as the operating point is moved from *edge-of-saturation* to *deep saturation*? What is the value of the ratio I_C/I_B when $v_W = 10\text{ V}$? How does it compare with β_F? Justify the designation β_{forced} for the ratio I_C/I_B when operation is past the *edge-of-saturation*.

Common-Emitter Amplifier:

With power off, assemble the circuit of Fig. 5 (implement R_E with $2 \times 10\text{-k}\Omega$ resistors in series), keeping the leads short and bypassing the power supply busses with 0.1-μF capacitors, as recommended in Appendix A2. Since the input v_i must be a small signal in order for the BJT to operate approximately linearly, we interpose a voltage divider R_1 and R_2 between the input source and the BJT to suitably scale down the source. With the resistor values shown we have $v_i \cong v_s/100$.

C7: Assuming v_s has DC value of 0 V in Fig. 5, predict the DC voltages V_B, V_E, and V_C at the base, emitter, and collector terminals, as well as the small signal gain $A_v = v_o/v_i$.

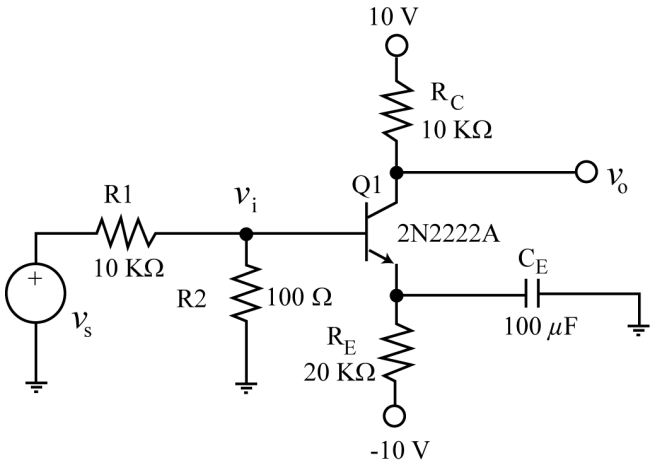


Fig. 5 - Common-Emitter amplifier.

M8: While monitoring v_s with Ch.1 of the oscilloscope (DC mode, Trigger from Ch. 1), adjust the signal generator so that v_s in Fig. 5 is a 10-kHz sinewave with 0-V DC and 1-V peak amplitude (this makes v_i a 10-mV peak amplitude sinewave). Next, use CH. 2 (DC mode, Chop Mode), to measure the DC voltages at the base, collector, and emitter pins; finally, switch Ch. 2 to the AC mode and measure the peak amplitude of v_o; hence, find the gain $A_v = v_o/v_i$ of your amplifier.

S9: Simulate the circuit of Fig. 5 using PSpice. For an effective simulation, you need to create a PSpice model for your specific BJT sample,

```
.model our_BJT npn (IS=Ival BF=Bval VAF=Vval)
```

where `Ival`, `Bval`, and `Vval` are the (most dependable) values of I_S, β_F, and V_A as found experimentally above. To invoke your transistor, you then use a command of the type: QXXX `C B E our_BJT`.

C10: Compare the predicted values of Step C7 with the measured values of Step M8 and the simulated values of Step S9; account for possible discrepancies.

M11: Returning to the circuit of Fig. 5, switch Ch. 2 back to the DC mode (make sure you know where your 0-V baseline is on the screen!), change the input generator's waveform from sinusoidal to triangular, and rise its

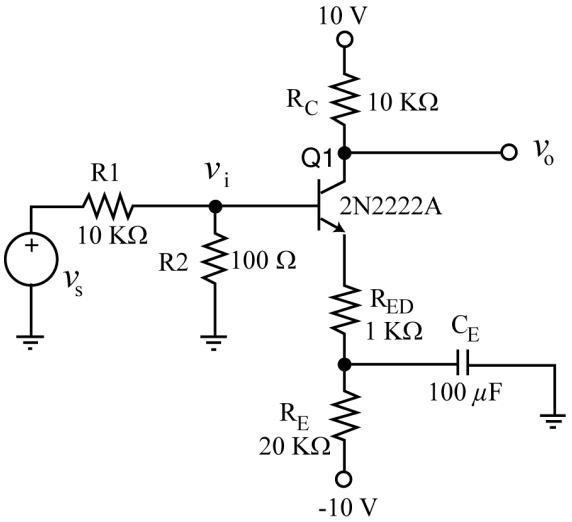


Fig. 6 - CE amplifier with emitter degeneration.

amplitude until v_o first begins to distort, then until it clips both at the top and at the bottom (in case the generator's maximum amplitude is not large enough, you my have to remove R_2 from your circuit). What causes distortion to occur? What are the values of the upper and lower clipping voltages? Justify the two clippings in terms of transistor operation.

CMS12: With power off, insert a 1-kΩ emitter degeneration resistor as shown in Fig. 6. Then, repeat Steps C7, M8, S9, and C10 for this new circuit. Hence, justify and verify the following well known rule of thumb: the gain of a *CE amplifier with emitter degeneration* is $A_v \cong R_C/R_{ED}$.

Common-Collector Amplifier:

With power off, assemble the circuit of Fig. 7, keeping leads short and using 0.1-μF power supply bypass capacitors, as usual. Then, adjust the input source so that v_s is a 10-kHz sinewave with 0-V DC and 5-V of peak-to-peak amplitude.

CMS13: Assuming v_s has DC value of 0 V in Fig. 7, predict the DC voltages V_B and V_E, as well the small signal gain $A_v = v_o/v_i$. Next, measure V_B, V_E, and A_v. Next, find V_B, V_E, and A_v via PSpice. Finally, compare the three sets of values, and account for possible discrepancies. *Note*: In this circuit, v_s has 5-V peak-to-peak amplitude, hardly a small signal; show that the BJT is nevertheless still operating under small signal conditions!

M14: In the circuit of Fig. 7 connect a load resistance $R_L = 10$ kΩ between the output and ground. Is the amplitude of v_o affected appreciably? Justify your findings! Next, with R_L in place, increase the amplitude of v_s (while leaving its DC value at 0 V) until v_o begins to clip at the bottom. At what voltage level does v_o clip? What causes this clipping to occur? *Hint:* What happens to v_o if you remove R_L from your circuit?

Current Source: One of the most popular applications of BJTs is as *current sources* (*pnp* BJTs) or *current sinks* (*npn* BJTs); in either case the output current is the collector current, thanks to the high resistance presented by this terminal. In the current source example of Fig. 8, D_1 establishes a reference voltage for biasing the BJT, and R_E establishes the output current as

$$I_O = (V_Z - V_{EB(\text{on})})/R_E$$

MC15: Mark one of your 2N3906 BJTs, and use the curve tracer to estimate its Early voltage V_A. *Note*: The estimation of V_A is similar to that of Step M1, except that you now need to adjust the POSITION knobs so that the origin of the *i-v* characteristic is at the *upper right* corner of the CRT; moreover, you must switch the POLARITY knobs from + to - both in the BASE STEP GENERATOR and the COLLECTOR SWEEP controls.

Once you have V_A, estimate the output resistance R_o of the current source of Fig. 8 as seen by the load; do your estimation for for the case $I_O = 1.0$ mA

M16: With power off, assemble the circuit of Fig. 8, keeping leads short and using a 0.1-μF power supply bypass capacitor, as usual. Then, with the multimeter configured as a digital current meter (DCM) and using first a wire as a load, turn on power and adjust the pot for $I_O = 1.0$ mA. Next, turn power off, insert a 3.0-kΩ load, and turn again

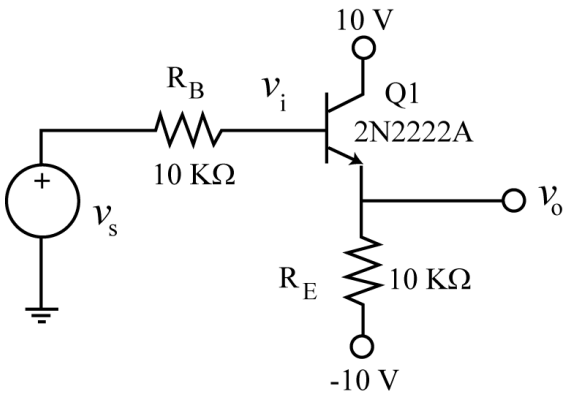


Fig. 7 - Voltage follower.

power on: does I_O change appreciably in spite of the 3-V change in the load voltage V_L? Justify in terms of the output resistance R_o estimated in Step. MC15.

MC17: Now rise the supply voltage from 10 V to 15 V while monitoring I_O with the DCM. By how much does I_O change? Justify quantitatively in terms of the zener diode model!

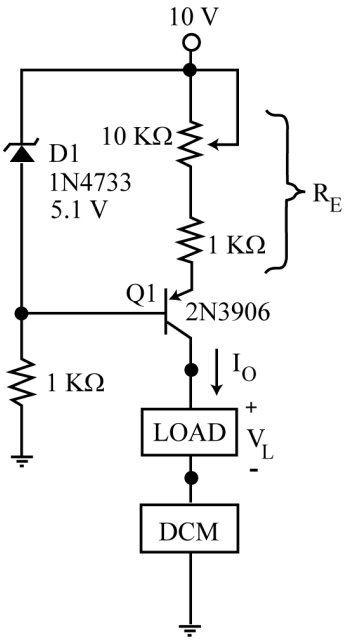


Fig. 8 - A pnp BJT as a current source.