ENGR 301 – Electrical Measurements

Experiment # 2: Operational Amplifier Characteristics

Objective:
To measure some of the most important parameters at the basis op amp limitations: the input pin *currents* I_P and I_N, the *input offset voltage* V_{OS}, the *common mode* and *power supply rejection ratios CMRR* and *PSRR*, the open loop *DC gain* A_{OL0}, the open loop *bandwidth* f_b, the *transition frequency* f_t, the small signal *rise time* t_R, the *slew rate SR*, and the upper and lower output *saturation limits* V_{OH} and V_{OL}. To assess the faithfulness of the 741 *macromodel* available in PSpice.

Components:
2 × 741C op amps, a 10-kΩ potentiometer, 3 × 0.1-μF capacitors, and miscellaneous resistors: 2 × 100 Ω, 2 × 10.0 kΩ, 6 × 100 kΩ, and 2 × 1.0 MΩ (all 1%, ¼ W).

Instrumentation:
A dual ±15-V regulated power supply, a signal generator (sinewave and squarewave), a digital multimeter, and a dual-trace oscilloscope.

References:

1. Sedra, Adel S., and Smith, Kenneth C., *Microelectronics*, 4th Ed, Oxford University Press, 1997.
2. Roberts, Gordon W., and Sedra, Adel S., *SPICE*, 2nd Ed., Oxford University Press, 1997.

Theoretical Background:
Ideally, an op amp has infinite open loop gain regardless of frequency, it draws zero currents at its input pins, and it can provide any voltage or current at its output pin.

In a practical op amp, the open loop gain is not only finite, but it rolls off with frequency. Moreover, the input pins draw tiny currents I_P and I_N, where the labels *P* and *N* denote, respectively, the *non-inverting* and the *inverting* input pins. If we tie the input pins together so that $v_N = v_P$, we expect the output v_O to be zero. In practice v_O will be different from zero, and if we wish to drive it to zero, a tiny corrective voltage must be applied between the input pins, called the *input offset voltage* V_{OS}. The parameters I_P, I_N, and V_{OS} are referred to as *DC imperfections*.

The mean of the two input pin currents is called the *input bias current* I_B, and their difference is the input *offset current* I_{OS}, or

$$I_B = (½)(I_P + I_N) \qquad\qquad I_{OS} = I_P - I_N \qquad (1)$$

The data sheets of the popular 741C op amp report the following typical (maximum) room temperature values: I_B = 80 nA (500 nA), I_{OS} = 20 nA (200 nA), and V_{OS} = 2.0 mV (6.0 mV). Note that I_{OS} and V_{OS} may be positive or negative, depending on the direction of imbalance.

At low frequencies the open loop gain A_{OL}, though not infinite, is still fairly large. This gain is aptly called the *DC gain* and is denoted as A_{OL0}. For the 741C op amp, A_{OL0} = 200,000 V/V typical, 50,000 V/V minimum. An op amp provides this high gain only up to some frequency called the *open loop gain bandwidth* f_b, after which gain rolls with frequency until a frequency f_t is reached at which gain becomes unity. Above f_t gain is less than unity; hence, f_t is called the *transition frequency*. The 741C op amp typically has $f_b \cong$ 5 Hz and $f_t \cong$ 1 MHz. For most op amps, including the 741 type, gain rolls off at a constant rate of –20 dB/dec, indicating that the open loop gain $A_{OL}(jf)$ can be expressed mathematically as

$$A_{OL}(if) = \frac{A_{OL0}}{1 + jf / f_b} \qquad (2)$$

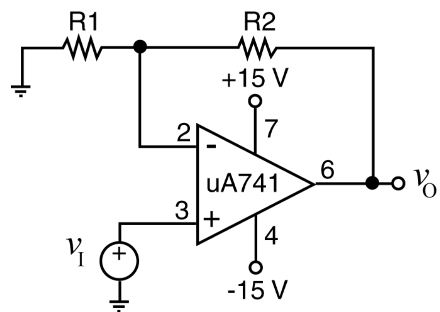

Fig. 1 - Noninverting Op-Amp configuration.

For the 741C op amp, $A_{OL}(jf) = 200{,}000/[1 + jf/(5\text{ Hz})]$ V/V. The *gain bandwidth product* is defined as GBP = $|A_{OL}| \times f$. For an op amp with a gain rolloff of –20 db/dec, this product is constant for $f \gg f_b$, namely, GBP = f_t.

The AC responses of op amps can readily be visualized via PSpice using suitable op amp models called *macromodels*. The file `Eval.lib` that comes with the student version of PSpice contains a 741 macromodel that is invoked via a command of the type

XOA vP vN VCC VEE vO ua741

Where vP, vN, VCC, VEE, and vO denote the nodes corresponding to the noninverting input, inverting input, positive supply, negative supply, and output. The following PSpice code is used to display the open loop frequency response of the 741 macromodel, as well as the closed loop frequency response of the non-inverting configuration of Fig. 1 for the case R_1 = 100 Ω and R_2 = 100 kΩ, or $\beta = R1/(R1 + R2) = 1/1001$ V/V. The statement `.lib eval.lib` tells PSpice where to look for the 741 macromodel.

```
741 Frequency Response
.lib eval.lib
VCC 7 0 dc 15V
VEE 4 0 dc -15V
Vi 3 0 ac 1mV
Ri 3 0 1k
R1 0 2 100
R2 2 6 100k
XOA 3 2 7 4 6 ua741
.ac dec 10 1Hz 10megHz
.probe
.end
```

The open loop and closed loop response are shown in Fig. 2.

If we operate a constant GBP Op-amp in the negative feedback mode with a constant feedback factor β, its

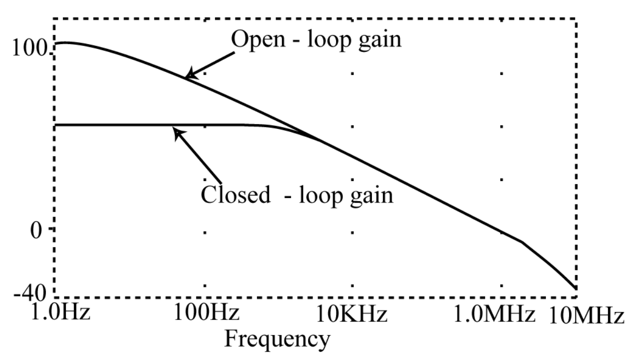

Fig. 2 – Open loop and closed loop response of the noninverting Op-amp configuration.

response to a sufficiently small step is an exponential transient characterized by the time constant $\tau = 1/2\pi\beta f_t$. The amount of time it takes for this transient to swing from 10% to 90% of its final vale is called the *rise time* t_R. It is readily seen that $t_R = \tau \ln 9 = 0.35/\beta f_t$. For instance, a 741C op amp connected as a voltage follower ($\beta = 1$) has $t_R = 0.35/f_t = 350$ ns. If the amplitude of the input step is gradually increased, a point is reached at which the output becomes slew rate limited, and the initial portion of the transient is a *ramp*. The slope of this ramp is called the *slew rate* (*SR*). For the 741C op amp, $SR \cong 0.5$ V/µs.

The following PSpice code is used to display the pulse response of the 741 macromodel for the noninverting configuration of Fig. 1 with $R_1 = 10$ k Ω and $R_2 = 100$ kΩ, or $\beta = R_1/(R_1 + R_2) = 1/11$ V/V.

```
741 Pulse Response (Small-Signal)
.lib eval.lib
VCC 7 0 dc 15V
VEE 4 0 dc -15V
vI 3 0 pulse (0 5mV 10ns 10ns 10ns 10us 20us)
Ri 3 0 1k
R1 0 2 10k
R2 2 6 100k
XOA 3 2 7 4 6 ua741
.tran 10ns 30us UIC
.probe
.end
```

As shown in Figure 3, the small signal pulse response consists of exponential transients, just like in the case of an ordinary *RC* network of the type investigated in ENGR 206. However, changing the parameters as in the following PSpice code,

```
741 Pulse Response (Large-Signal)
.lib eval.lib
VCC 7 0 dc 15V
VEE 4 0 dc -15V
Vi 3 0 pulse (0 1V 100ns 100ns 100ns 50us 100us)
Ri 3 0 1k
R1 0 2 10k
R2 2 6 100k
XOA 3 2 7 4 6 ua741
.tran 100ns 120us UIC
.probe
.end
```

results in the large signal pulse response shown in Fig. 4, characterized by slew rate limited ramps.

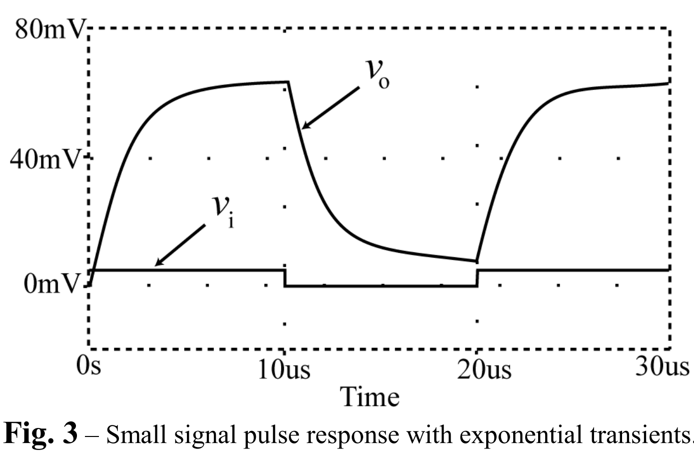

Fig. 3 – Small signal pulse response with exponential transients.

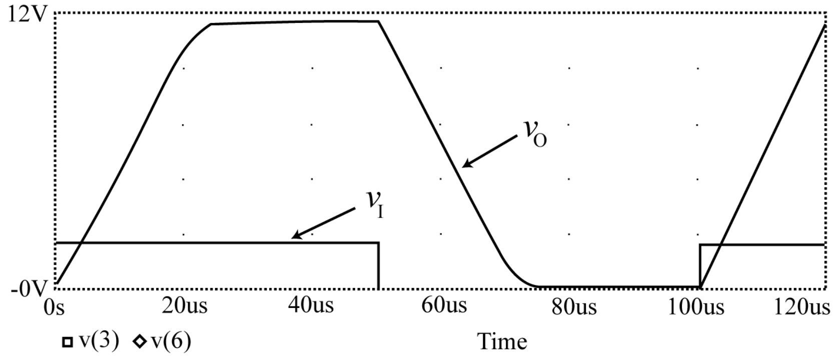

Fig. 4 – Large signal pulse response.

Experimental Setup:

Most measurements shall be performed using the circuits of Figs. 5 and 6, which each lab group should assemble simultaneously in separate areas of the protoboard before coming to the lab. This will allow using the allotted lab time efficiently, primarily to perform the required measurements and observations. Please refer to Appendix 2 for useful tips on how to construct op amp circuits. In particular, use two 0.1-μF capacitors to bypass the ±15-V power supplies, and always turn off power before making any changes in a circuit. Failure to do so may destroy the op amp, indicating that all measurements performed up to that point will have to be repeated!

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, and **S** for SPICE simulation. Moreover, each measured value should be expressed in the form $X \pm \Delta X$ (e.g. V_{OS} = 1.5 mV ± 0.1 mV), where ΔX represents the estimated uncertainty of your measurement, something you have to figure out based on your learning in ENGR 300.

DC Parameters:

In the circuit of Fig.5, the op amp at the left is the *device under test* (DUT), and the op amp at the right provides a servo loop to force the output of the DUT near 0 V and all possible test conditions. Also, note that to simplify inventory, we implement the 50.0-kΩ resistance by connecting two 100-kΩ in parallel.

C1: Show that with the given component values, the circuit of Fig. 5 yields

$$v_2 = 500(R_pI_P - R_nI_N - V_{OS} - v_1/A_{OL}) \qquad (3)$$

where I_P and I_N are the input pin currents of the DUT, assumed to be flowing into the DUT, and V_{OS} and A_{OL} are the input offset voltage and open loop gain of the DUT. The switches shown are ordinary wires that are used to selectively short out the corresponding resistors and thus force one or more of the terms in Eq. (3) to vanish.

M1: With both SW_1 and SW_2 closed and v_1 = 0 V (ground), measure v_2 with he digital voltmeter (DVM). Hence, use Eq. (3) to find V_{OS}.

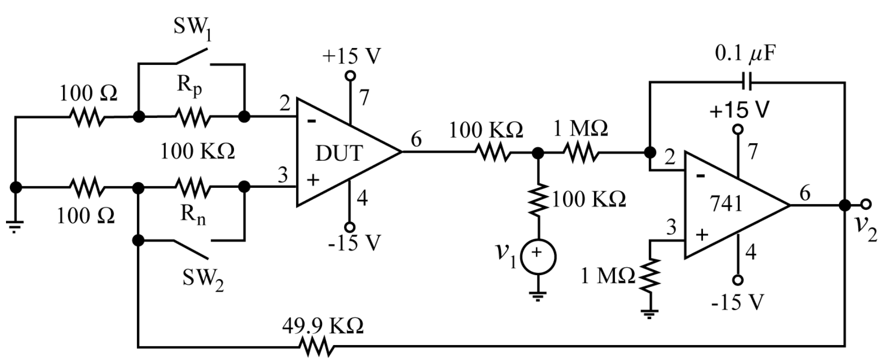

Fig. 5 – Experimental setup to measure DC parameters.

M2: With SW_1 closed, SW_2 open, and v_1 = 0 V (ground), measure v_2 with the (DVM). Hence, use Eq. (3), along with the result of Step M1, to find I_P.

M3: With SW_1 open, SW_2 closed, and v_1 = 0 V (ground), measure v_2 with the (DVM). Hence, use Eq. (3), along with the result of Step M1, to find I_N.

M4: With both SW_1 and SW_2 closed and v_1 = 15 V (use the +15-V supply) , measure v_2 with the (DVM). Hence, use Eq. (3), along with the result of Step M1, to find A_{OL0}.

C5: Using Eq. (1), calculate I_B and I_{OS}. Hence, compare your values of I_B, I_{OS}, V_{OS}, and A_{OL0} with those given in the data sheets. Comment.

M6: With both SW_1 and SW_2 closed and v_1 = 0 V (ground), lower the positive supply V_{CC} from +15 V to +10 V while keeping V_{EE} = -15 V. Measure with the DVM the resulting variation in v_2 , and hence calculate the corresponding change ΔV_{OS}. Finally, calculate the *positive power supply rejection ratio* as
$PSRR_p = 20 \ln |\Delta V_{CC} / \Delta V_{OS}|$.

M7: Repeat Step M5, except that now you keep V_{CC} = +15 V and change V_{EE} from –15 V to –10 V. The result is now the *negative power supply rejection ratio* as $PSRR_n = 20 \ln |\Delta V_{EE} / \Delta V_{OS}|$. Compare the two *PSRR*s, comment.

Offset Nulling:

For the next set of measurements we use the circuit of Fig. 6 with $R_1 = R_4 = 100\ \Omega$ and $R_2 = R_3 = 100\ \text{k}\Omega$. Given the high closed loop gain (1001 V/V), the input v_I must be kept suitably small to avoid saturation effects at the output, so we use an input voltage divider, as shown. Since the resistances of the divider are the same as those in the feedback network, the overall low frequency gain from v_S to v_O is nominally unity. Initially, the 10-kΩ potentiometer is left out of the circuit.

C8: Ignoring the 10-kΩ pot in the circuit of Fig. 6, use the results of your previous measurements to predict the value of v_O with v_S = 0 V (ground). Next, apply power but without connecting the 10-kΩ potentiometer yet, and measure v_O with the DVM. How does it compare with the predicted value? Comment.

Next, turn off power, connect the 10-kΩ pot in the manner shown, reapply power, and adjust its wiper until v_O comes as close as possible to 0 V. The purpose of the pot is to deliberately imbalance the internal circuitry of the op amp so as to make it possible for us to drive v_O to zero. This action is referred to as *internal offset nulling*. Once the pot has been adjusted, it should not be touched again.

Frequency Response:

For this response, use still the circuit of Fig. 6 with $R_1 = R_4 = 100\ \Omega$ and $R_2 = R_3 = 100\ \text{k}\Omega$, and monitor v_S and v_O with Ch. 1 and Ch. 2 of the oscilloscope (both channels on DC, Trigger from Ch. 1, Chop Mode; make sure you know where the 0-V baselines of your traces are!) Adjust the signal generator so that v_S is a sinusoidal wave with a

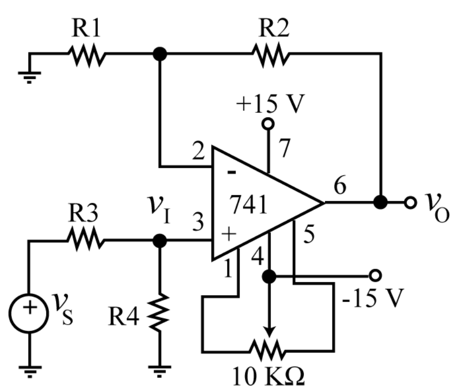

Fig. 6 - Circuit used for offset nulling.

1-V amplitude (2-V peak-to-peak) and 0-V DC offset.

M9: Starting at low input frequencies, increase frequency until the amplitude of v_O drops to 0.707 of its low frequency value. This frequency is the –3-dB frequency f_{-3dB}, which is related to the transition frequency f_t as $f_{-3dB} = \beta f_t$.

M10: Measure the amplitude of v_O also at $10f_{-3dB}$ and $100f_{-3dB}$, and verify the constancy of the *GBP*. Hence, estimate f_t.

C11: Using the value of A_{OL0} obtained in step M4, estimate f_b. Hence, sketch the magnitude Bode Plots of both the open loop and closed loop responses of the circuit of Fig. 7.

S12: Rerun the `741 Frequency Response` PSpice program above, and use the cursor facility to determine A_{OL0}, f_b, f_t, and f_{-3dB}. Hence, compare with your measured values and comment on the quality of the 741 PSpice macromodel in the frequency domain.

Small-Signal Transient Response:

For this response use still the circuit of Fig. 6, but with $R_1 = R_4 = 10$ k Ω and $R_2 = R_3 = 100$ kΩ (make sure you turn power off as you change R_1 and R_4 from the previous step). Also, adjust the signal generator so that v_S is a squarewave alternating between 0 V and +55 mV.

M13: Adjust the input frequency so that the waveforms appear somewhat as in Fig. 3. Hence, using the techniques of ENGR 206, measure the rise time t_R. How does the measured value compare with the expected value $t_R = 0.35/\beta f_t$? Comment.

S14: Rerun the `741 Pulse Response (Small-Signal)` program above, and use the cursor facility to determine t_R. Hence, compare with your measured value and comment on the quality of the 741 PSpice macromodel in the time domain.

Large-Signal Response:

For this response, use still the circuit of Fig. 6, but with R_1 =10 k Ω, $R_2 = R_3 = 100$ kΩ, and R_4 removed from the circuit. Then, rise the input pulse amplitude to 1 V.

M15: Adjust the input frequency so that the waveforms appear somewhat as in Fig. 4. Hence, determine the slopes of the two ramps, in V/μs. How do they compare with the data sheet *SR* value for the 741C?

M16: Adjust v_S so that it is a 1-kHz sinewave alternating between about –1 V and +1 V. Then, gradually rise the amplitude of v_S until v_O clips. Measure on the oscilloscope the upper and lower saturation limits V_{OH} and V_{OL}. Are they symmetric? Different? Justify.

M17: Reduce v_S until the peaks of v_O are just a bit less than the saturation limits, say, 0.5-V less. Then, rise the input frequency until v_O just begins to distort near its zero crossings. This distortion is due to slew rate limiting, and the frequency corresponding to the onset of distortion is the *full power bandwidth* (*FPB*). Compare the measured value of *FPB* with the predicted value $FPB = SR/2\pi V_{om}$, where V_{om} is the peak amplitude of v_O; comment.

M18: Reduce v_S to half its value of Step M17, and find the new input frequency at which v_O just begins to distort near its zero crossings. Again, compare with the predicted value $FPB = SR/2\pi V_{om}$; comment.

The Voltage Follower

For this part, use still the circuit of Fig. 6, but with $R_2 = R_3 = 10$ kΩ, and R_1 and R_4 removed from the circuit, so that we now have a voltage follower.

MS19: Measure the frequency response, as well as the small signal and large signal pulse responses; simulate all three responses with PSpice; compare simulations and measurements; comment.

The Difference Amplifier and the CMRR:

For this part, use the circuit of Fig. 7, which is similar to that of Fig. 6, except that R_1 and R_2 are tied together and driven with a common signal v_S. For the variable resistance, use the 10-kΩ pot you used for offset nulling. Initially, assemble the circuit without the 2-MΩ resistance, and with the wiper all the way to the left, so that the variable resistance is 0 Ω. Make sure power is off as you assemble your circuit! Also, adjust v_S so that it is a 100-Hz sinewave with peak amplitude V_{im} = 5 V and O-V DC offset.

M20: With the 2-MΩ resistor initially disconnected and the wiper all the way to the leftt, measure the peak amplitude V_{om} of v_O. Then, calculate the *common mode* voltage gain $A_{cm} = V_{om}/V_{im}$, and hence, the *common mode rejection ratio CMRR* = 20 log $|A_{dm}/A_{cm}|$, where $A_{dm} = R_2/R_1$ is the *differential mode* gain.

M21: Turn power off, insert the 2-MΩ resistor (implement it by recycling the two 1-MΩ resistors of Fig. 5 and connect them in series), reapply power, and vary the wiper until v_O is minimized. This, in turn, maximizes the *CMRR* of the circuit. What is its new value, in dB?

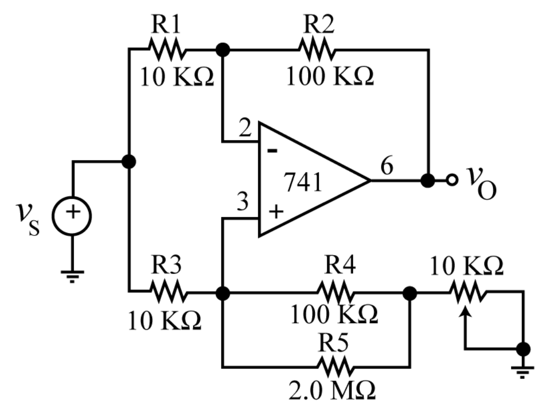

Fig. 7 - Circuit to investigate the difference amplifier and the CMMR.

APPENDIX 2: TIPS ON OP AMP CIRCUIT LAYOUT AND PRECAUTIONS

Unless otherwise specified, op amps shall be powered from V_{CC} = +15V and V_{EE} = -15V. Due to their extremely high gains, op amps are prone to oscillation. To prevent unwanted oscillations, you should systematically abide by the following rules:

1. Bypass the supply leads to the op amp towards ground by means of two good RF capacitors, such as 0.1- µF disc ceramic or 1.0µF tantalum capacitors.

2. Use minimum-length layouts. This applies especially to the op amp's inverting input lead in negative-feedback configurations.

3. If you need to observe the voltage at any one of the op amp's critical pins, particularly the inverting- input pin, by means of the oscilloscope or the DMM, avoid connecting the instrument's lead directly to the op amp's critical pin. Always place a series resistor, say 10 kΩ, between the two.

IC op amps are fairly delicate devices; as such they can easily be destroyed, unless suitable precautions are taken, as follows:

4. Whenever you need to make a circuit change, turn the power supplies off. After making your change, check once more for possible wiring errors before reapplying power.

5. To prevent damaging the op amp input stage, make sure the voltage you apply to either input terminal never exceeds $+V_{CC}$ and never goes below $-V_{EE}$; this happens, for instance, if the power supplies are turned off while the input signal generator is still on. To avoid damaging the input stage, it is a good idea to use a series resistance, say, 10 kΩ, between the signal generator and the input pin.

6. Don't connect anything to the op amp pins that are not in use.

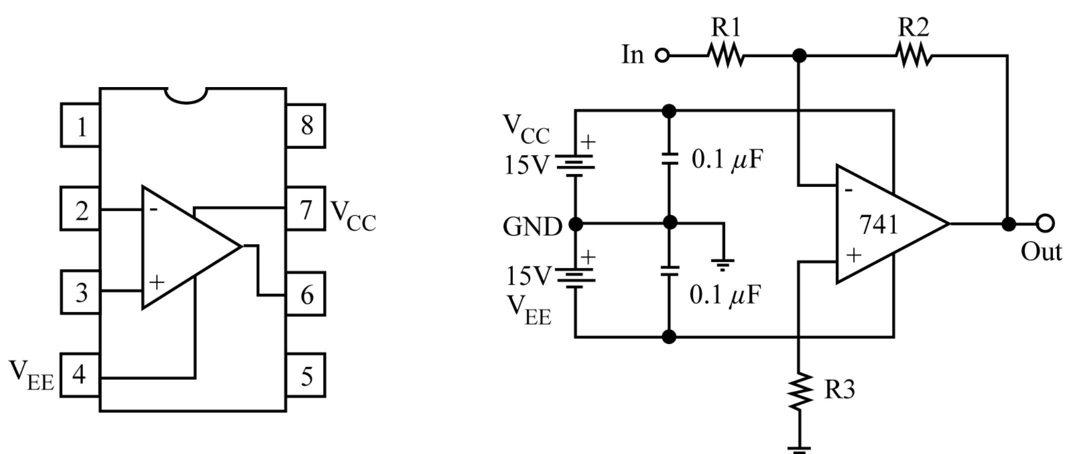

Fig. A2.1 - Pinout for the 741 op amp, and power-supply interconnection for the inverting configuration.

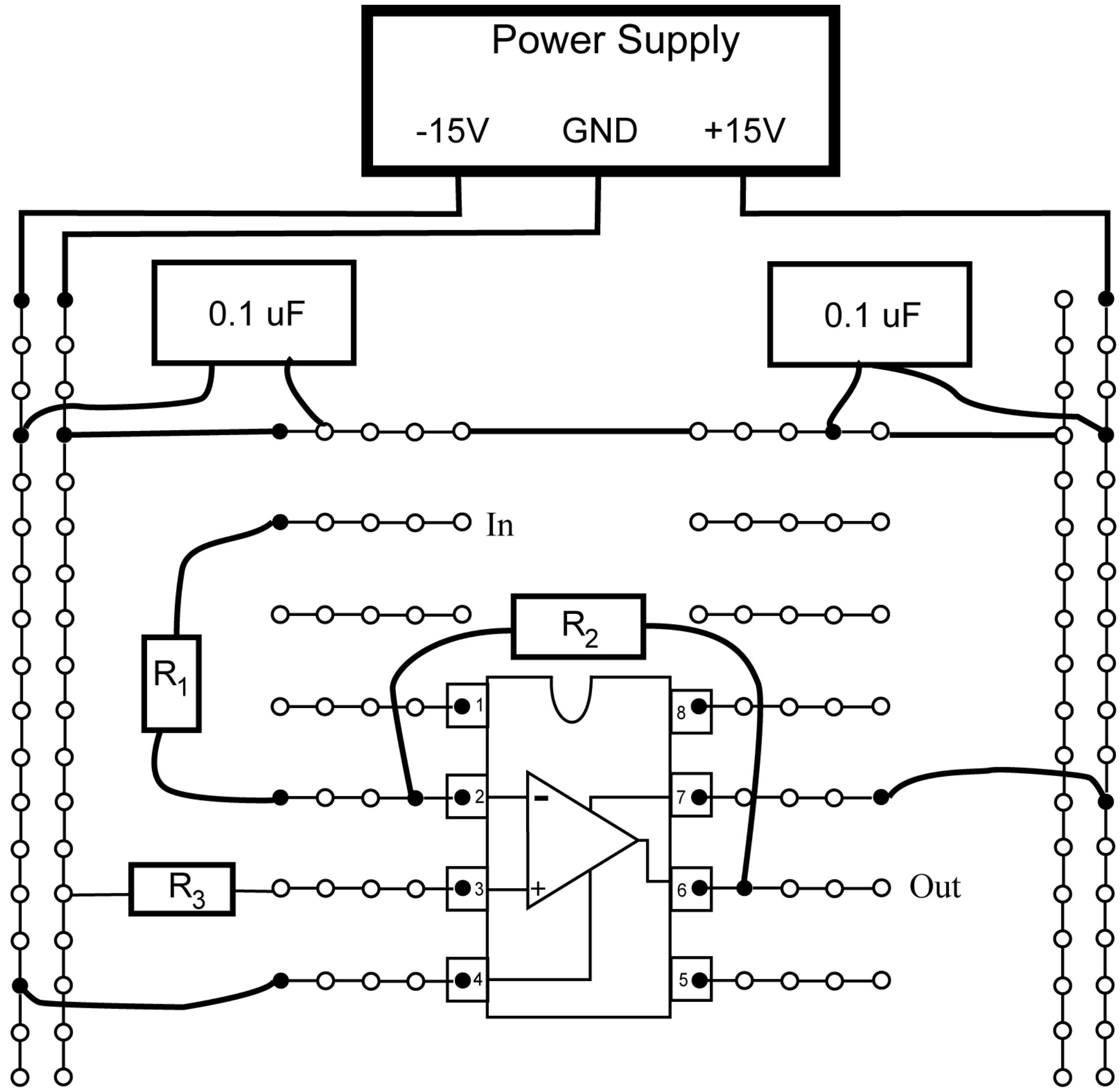

Fig. A2.2 -Recommended conventions and circuit layout for op amp circuits. The example refers to a µA741 connected as an inverting amplifier, but the features of this example should be applied to other circuits and op amps as well.